

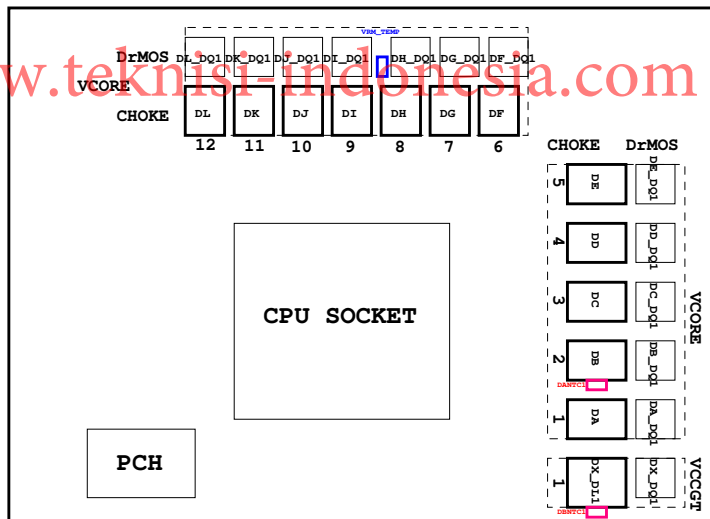
Model Name: B560M DS3H

SHEET TITLE rev 1.0

01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU_LGA1200-A	(RKL_R0.1)
05	CPU_LGA1200-B-DDR4	(RKL_R0.1)
06	CPU_LGA1200-C	(RKL_R0.1)
07	CPU_LGA1200-D	(RKL_R0.1)
08	DDR 4 CHANNEL A	(CML_R0.1)
09	DDR 4 CHANNEL B	(CML_R0.1)
10	PCH CLK,DMI,CNVI	(RKL_R0.1)
11	PCH SPI,USB	(RKL_R0.1)
12	PCH PCIE,SATA	(RKL_R0.1)
13	PCH ESPI,MISC	(RKL_R0.1)
14	PCH GPP,HDA	(RKL_R0.1)
15	PCH PWR,GND	(RKL_R0.1)
16	Heatsink	
17	ITE ITE8689	(RKL_R0.1)
18	HWM	(RKL_R0.1)
19	FAN CTRL-CFL-SIO_5 FAN	(RKL_R0.1)
20	Single BIOS for CS mode	(RKL_R0.1)
21	PCI EXPRESS X16 SLOT	(REV0.3)
22	PCI EXPRESS X4 SLOT(PCH)	(REV0.51)
23	PCI EXPRESS X1 *3	(REV0.51)
24	SATA	
25	M.2 x4 (A)	(RKL_R0.1)
26		(RKL_R0.1)
27		(RKL_R0.1)
28	M.2 x4 (P)	(RKL_R0.1)
29	COM,LPT,TPM, THB	(CML_R0.94)
30	ISL69269_L=0.15u	(RKL_R0.1)
31	RAA229001_L=0.15u	(RKL_R0.1)
32	VCORE_PSTAGE-1_L=0.15u	(RKL_R0.1)
33	VCORE_PSTAGE-2_L=0.15u	(RKL_R0.1)
34	VCORE_PSTAGE-3_L=0.15u	(RKL_R0.1)
35	VCCGT_PSTAGE_L=0.15u	(RKL_R0.1)
36	VCCSA_MOS	(RKL_R0.1)
37	VCCIO-Ferrite-Z系列	(RKL_R0.1)
38	VCCIO2-Ferrite-Z系列	(RKL_R0.1)
39	RT8120_DDR_CHOKE-Ferrite-2L	(RKL_R0.1)
40	RT8120_VPP_CHOKE-合金	
41	NCP81269_VCC18_PCH	
42	RT8068_VCC1V8_PRIM	
43	DISCRETE POWER	(REV0.1)
44	ATX POWER , A_-PROCHOT	
45	HDMI_NO LS	(CML_R0.94)
46	CNVi_M2_WIFI	(CML_R0.94)
47	Redriver_RTS5461_A	(RKL_R0.1)
48	RTS5441E_A_Type-C	(RKL_R0.1)
49	Redriver_RTS5461_B	(RKL_R0.1)

SHEET TITLE

50	R_USB30x4	(CML_R0.94)
51	GENESYS GL850S_1	(RKL_R0.1)
52	GENESYS GL850S_2	(RKL_R0.1)
53	F_USB20	(CML_R0.94)
54	F_U32	(CML_R0.94)
55	KB_MS_USB	(CML_R0.94)
56	RTS5441E_B_Front1	(RKL_R0.1)
57	INTEL I219	(CML_R0.3)
58	U32_LAN CONNECTOR-I219	(CML_R0.3)
59	Realtek ALC1200	(RKL_R0.6)
60	REAR AUDIO JACK	(RKL_R0.6)
61	CPU POWER-1	(RKL_R0.1)
62	CPU POWER-1	(RKL_R0.1)
63	NCT3933	
64	F_PANEL	
65	IT5702	(RKL_R1.0)
66	PCH/AUDIO/DEBUG/C_LED1/2	(RKL_R1.0)
67	D_LED1/D_LED2	
68	SMBUS SWITCH	(RKL_R0.1)
69	CKG	(RKL_R0.1)
70	EMI-ESD	
71	POWER MAP	
72	NTC MAP	

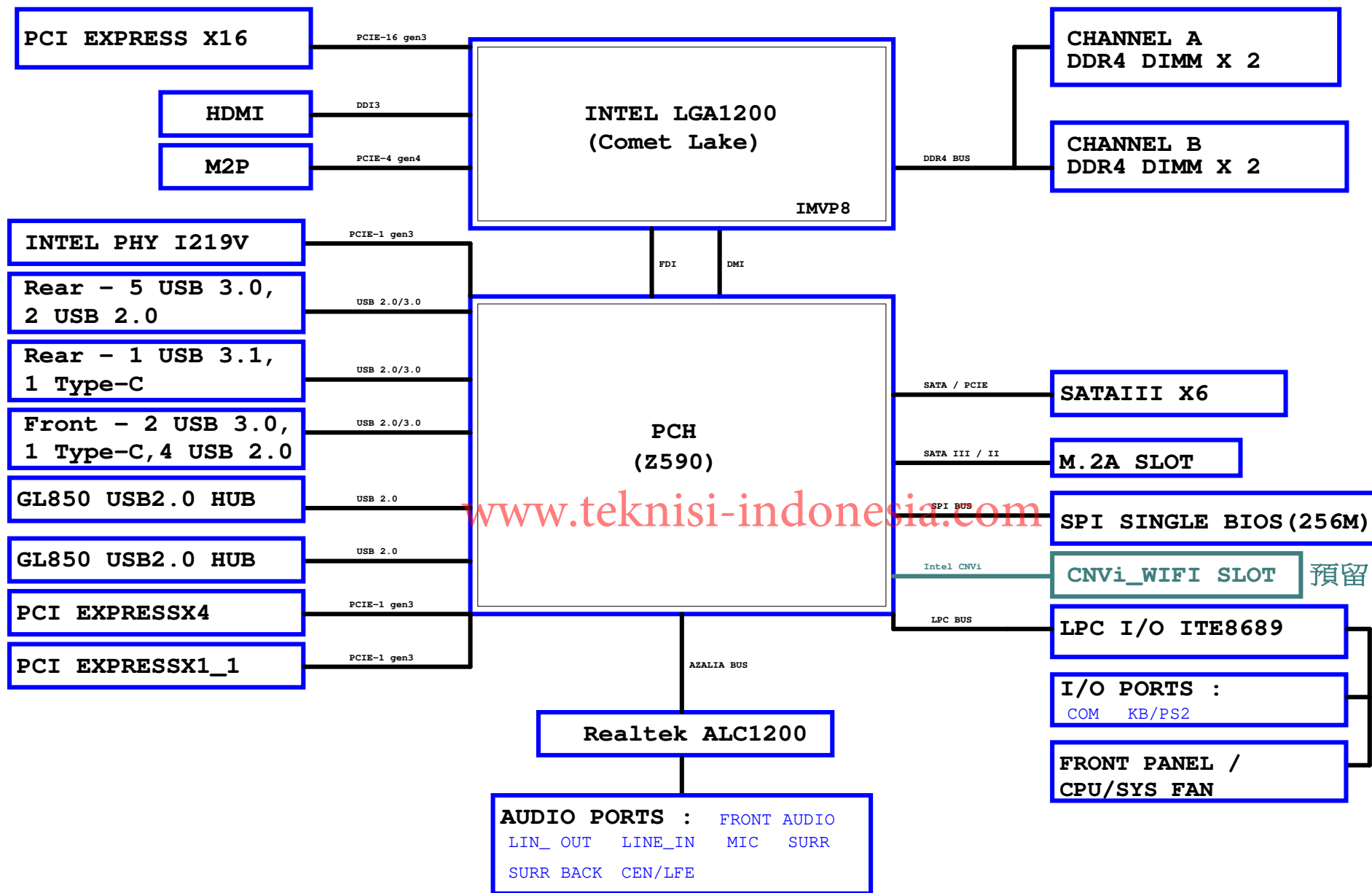


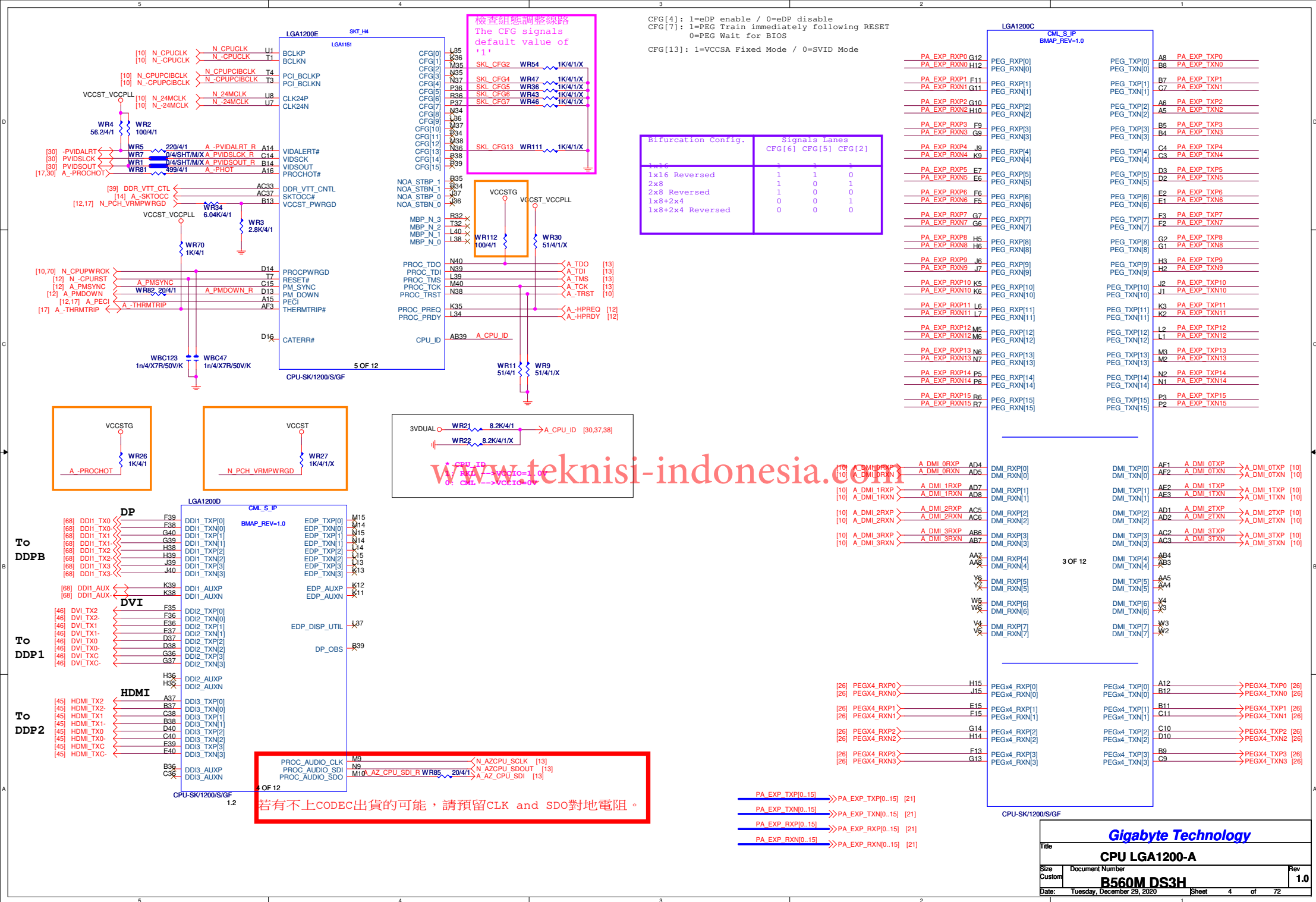
Circuit or PCB layout change

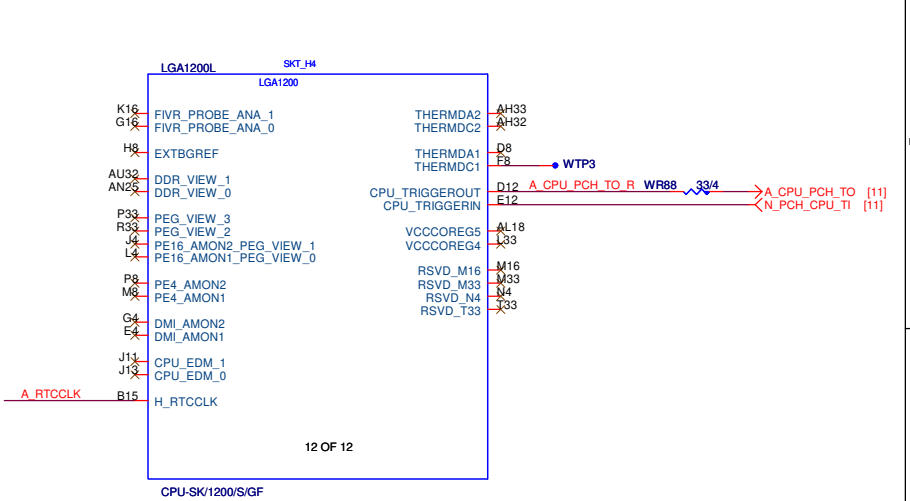
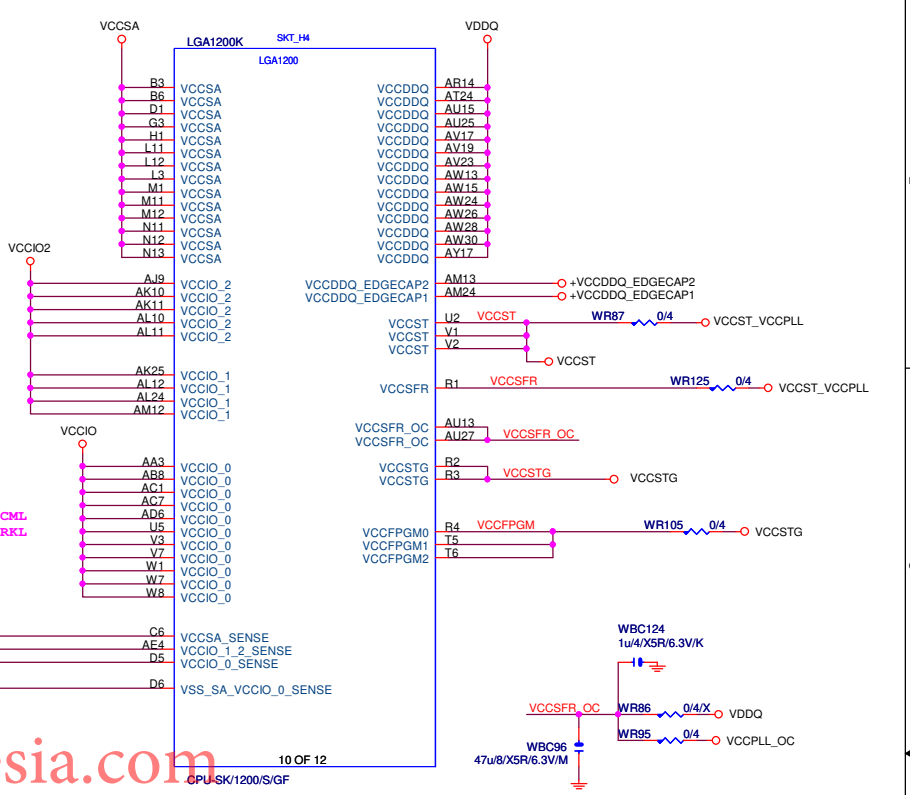
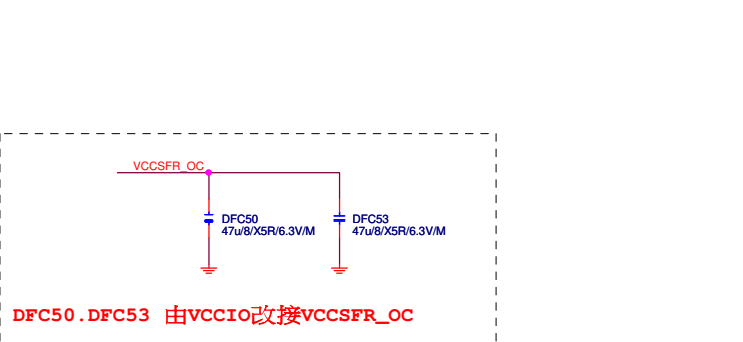
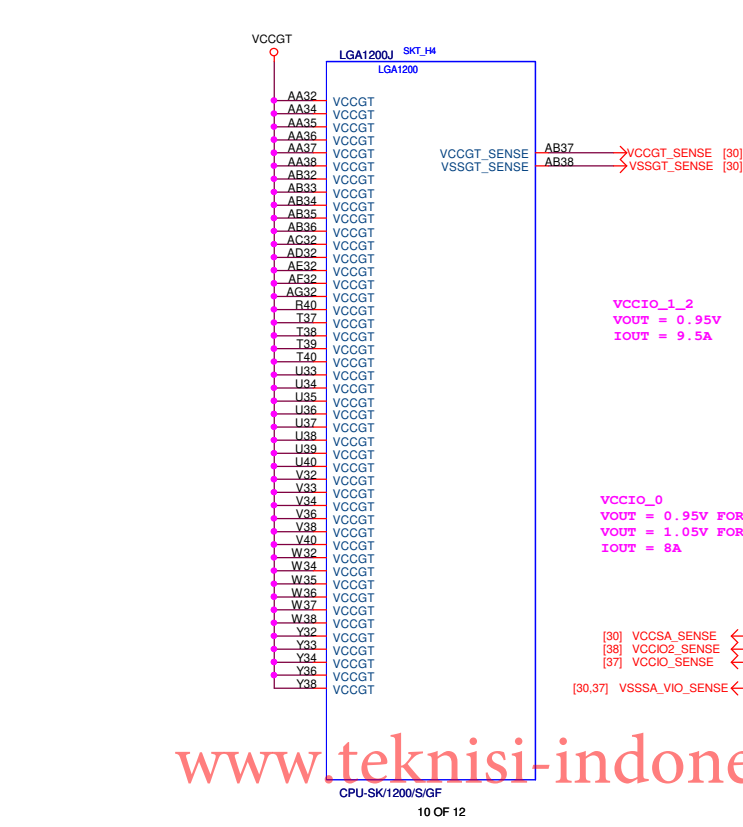
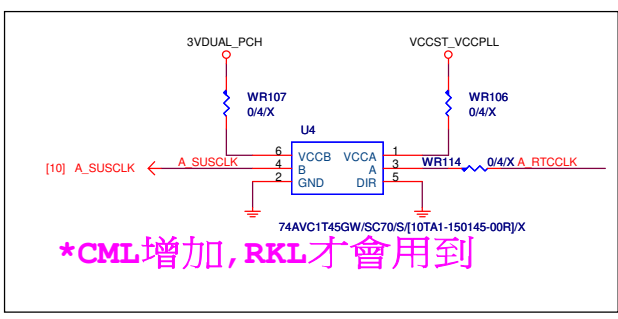
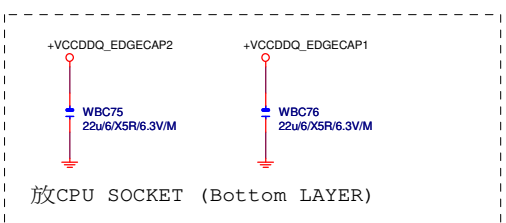
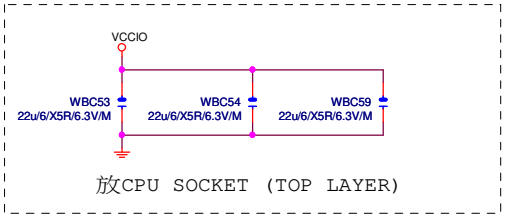
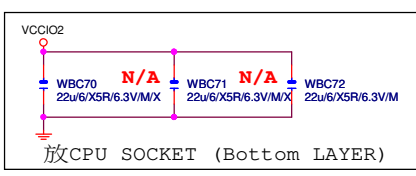
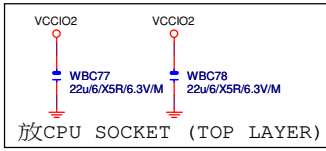
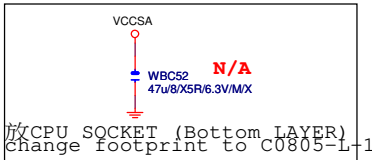
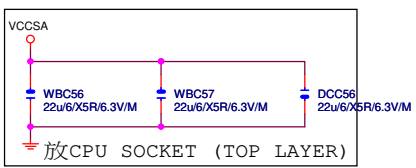
2020/12/17

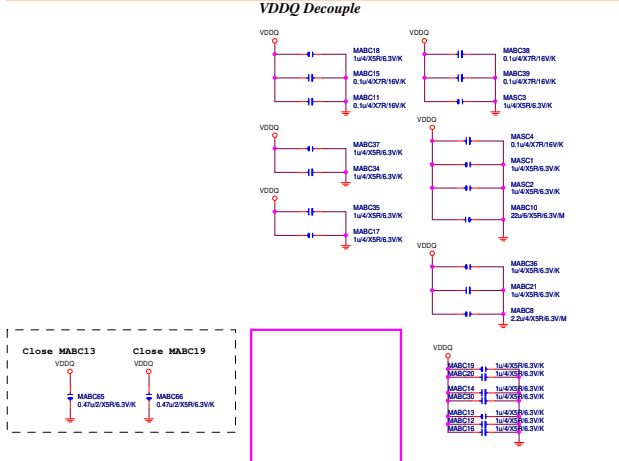
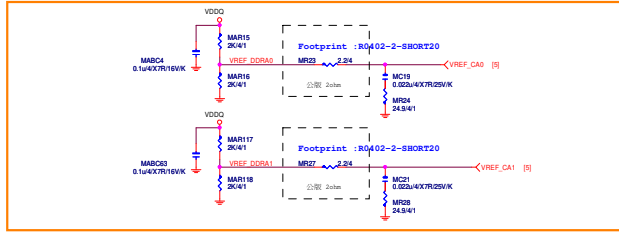
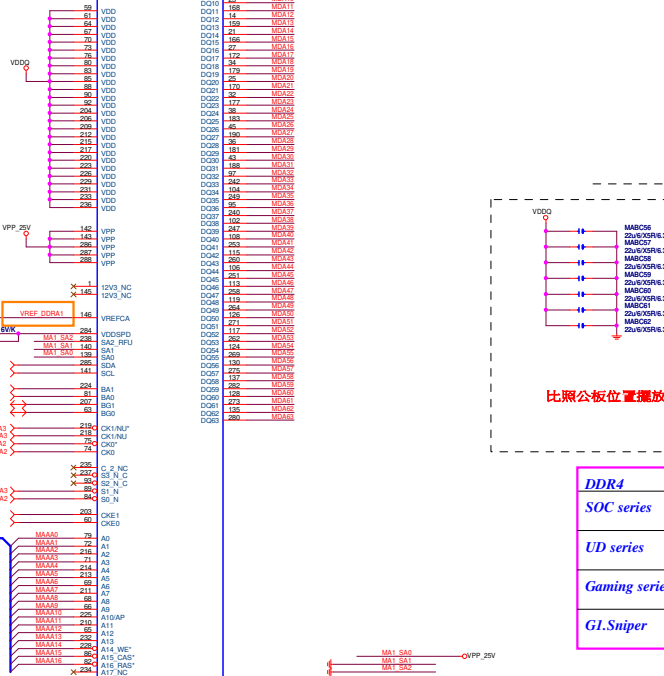
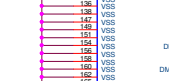
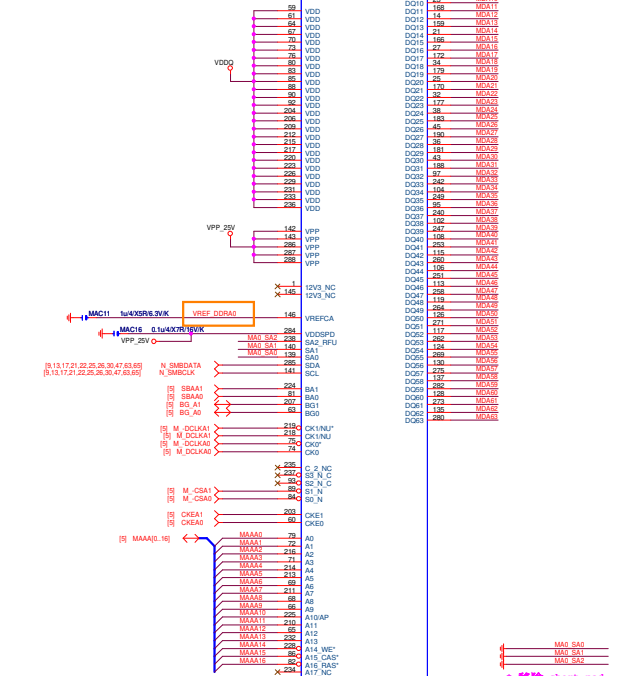
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BLOCK DIAGRAM

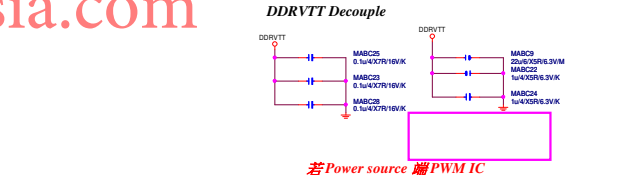




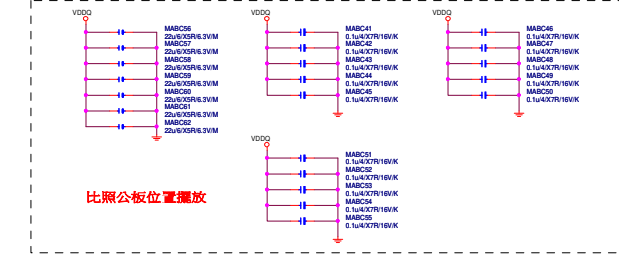




若Power source 端PWM IC
已有擺放,則可刪除



若Power source 端PWM IC
已有擺放,則可刪除

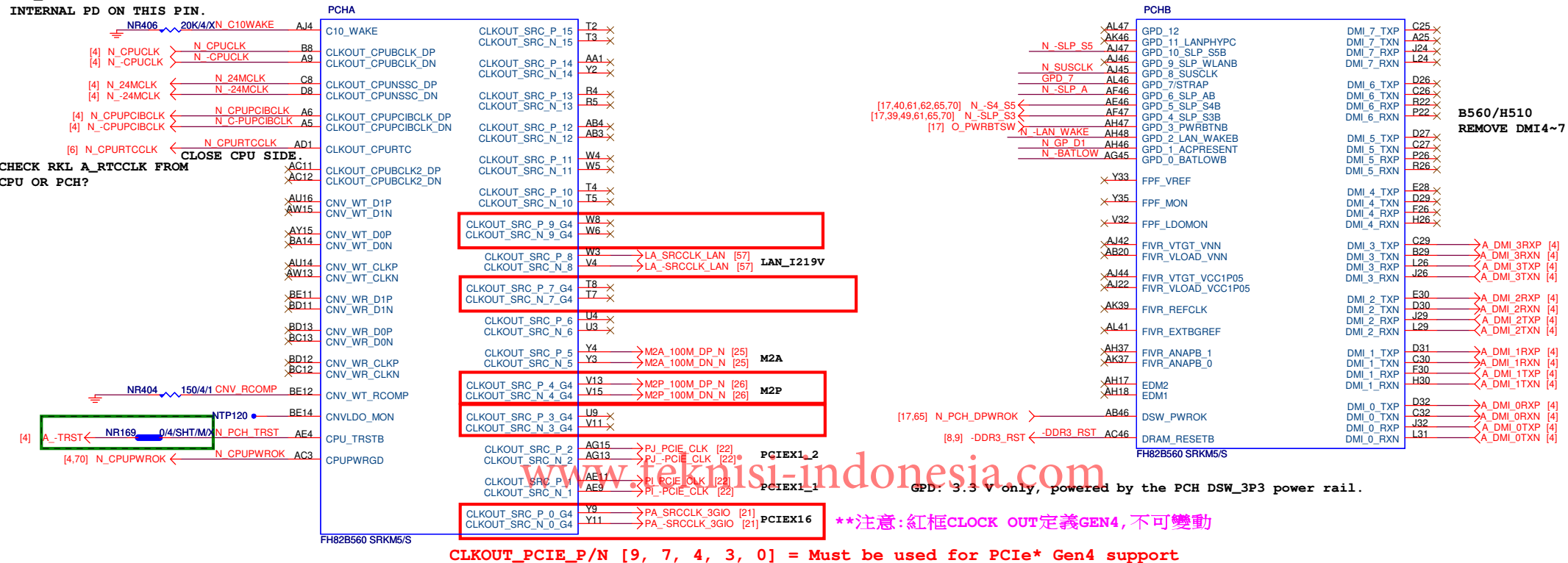


比照公板位置擺放

DDR4		Capture Value
SOC series	黑色 褐色	DDR4/288/BK/VA/S/G15/4ROW/LONG DDR4/288/OR/VA/S/G15/4ROW/LONG
UD series	黑色 深灰色	DDR4/288/BK/VA/D/G15/ONE LATCH/LONG DDR4/288/GY/VA/D/G15/ONE LATCH/LONG
Gaming series	黑色 鮮紅	DDR4/288/BK/VA/D/G15/ONE LATCH/LONG DDR4/288/RE/VA/D/G15/ONE LATCH/LONG
GL Sniper	黑色 綠色	DDR4/288/BK/VA/D/G15/ONE LATCH/LONG DDR4/288/GE/VA/D/G15/ONE LATCH/LONG

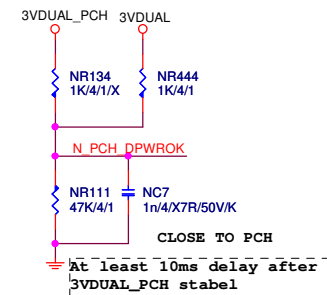
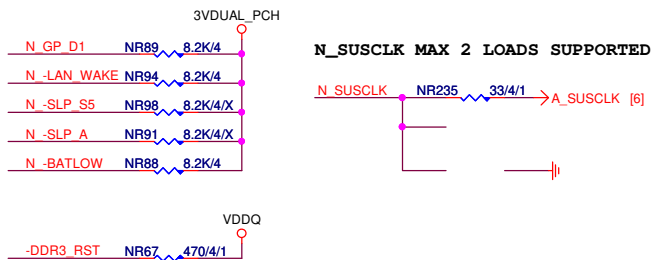
RKL_TGP_PCH-H R0.1

C10_WAKE RESERVED/BIOS NEED TO PROGRAM
INTERNAL PD ON THIS PIN.



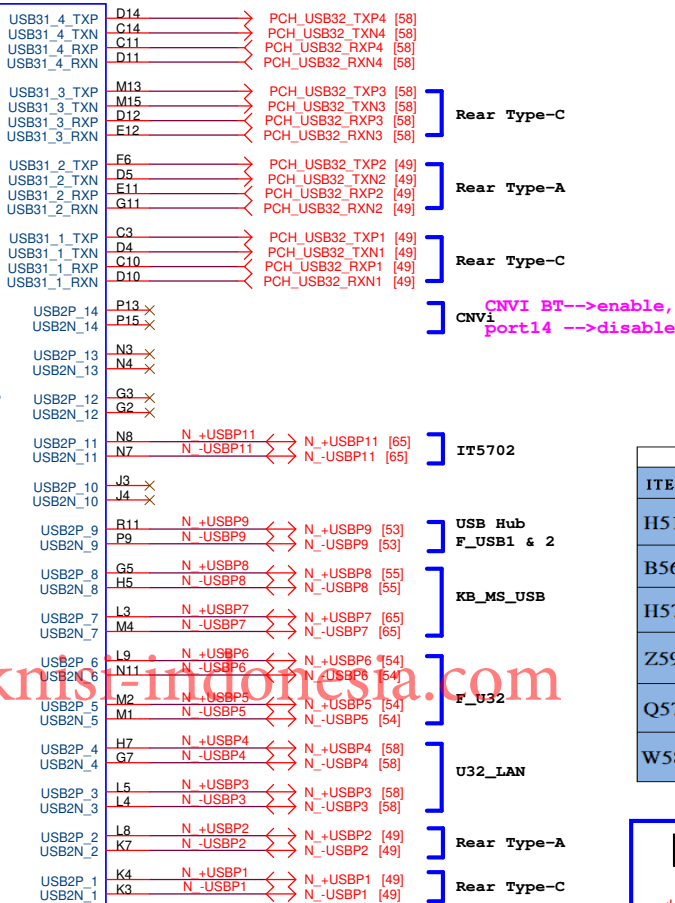
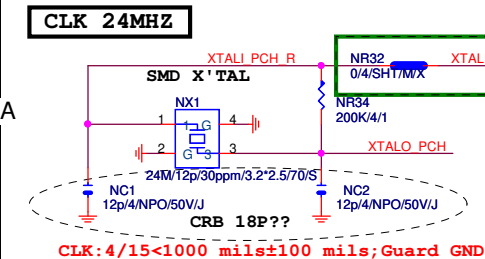
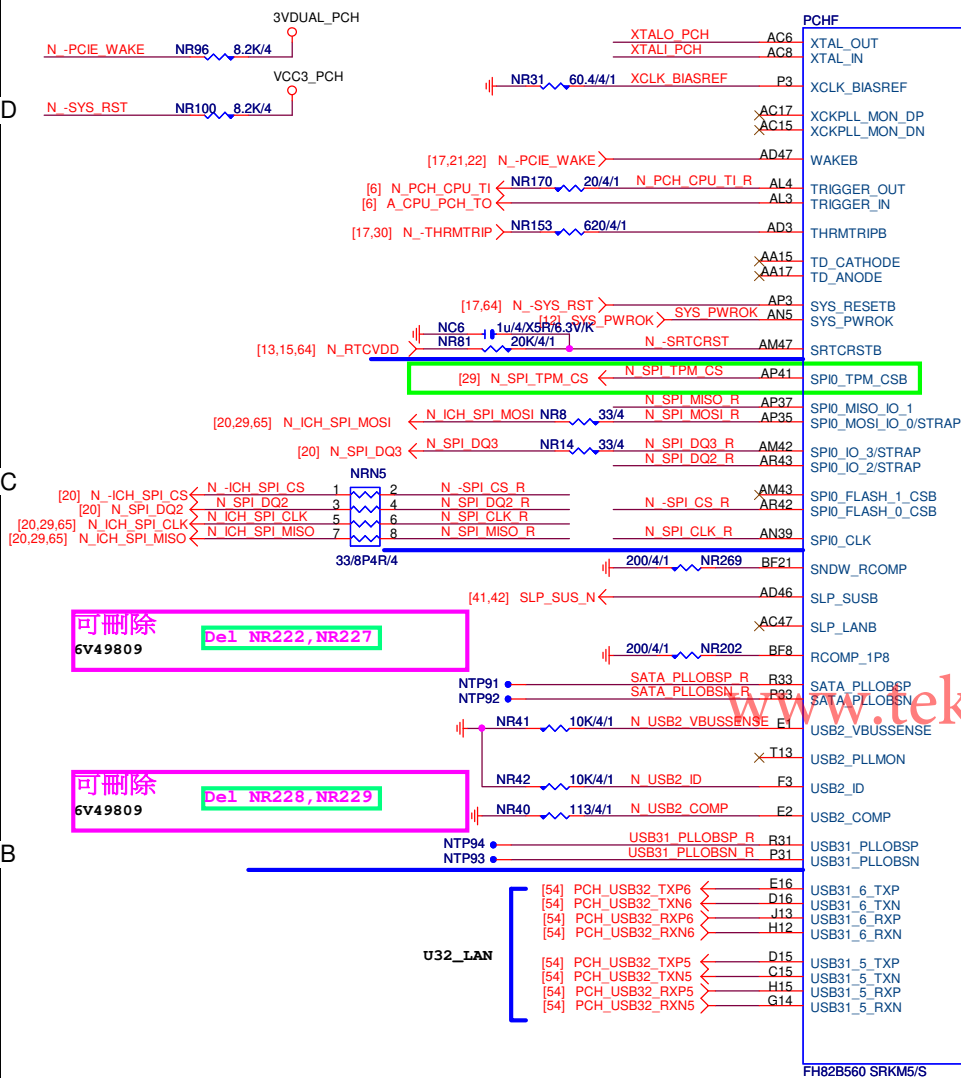
STRAP

3VDUAL_PCH
GPD 7 NR237 100K/4/X
Reserved. This strap should sample LOW INTERNAL PD.



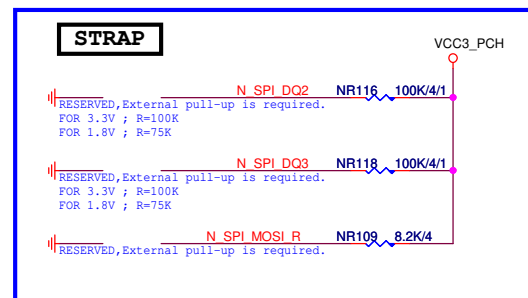
ANS	8594505	Gigabyte Technology
Title		
PCH CLK, DMI, CNVI		
Size	Document Number	Rev
B	B560M DS3H	1.0
Date:	Friday, January 22, 2021	Sheet 10 of 72

RKL_TGP_PCH-H R0.1

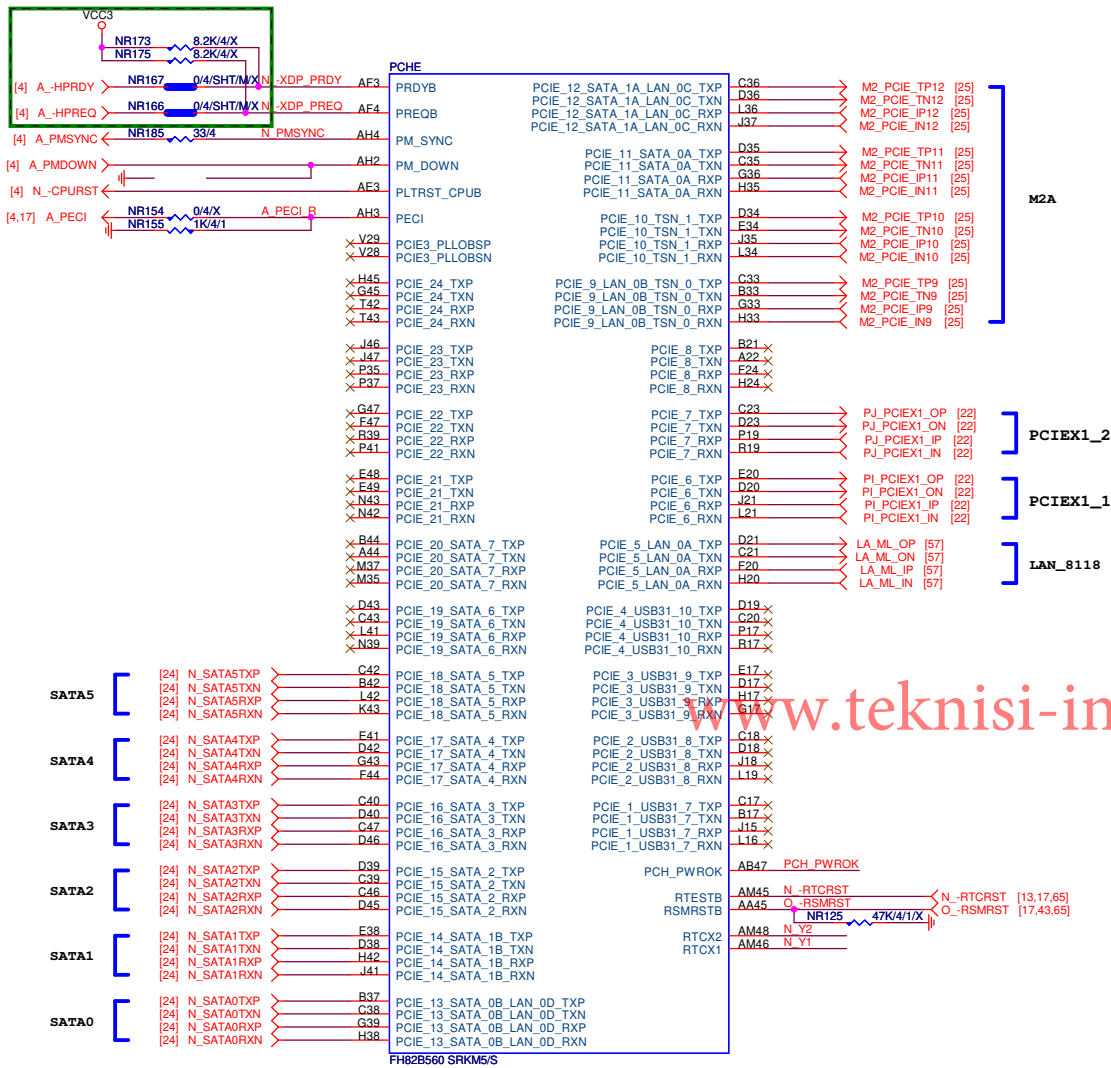


Intel 500 series PCH USB configuration P1~P6						
ITEM	USB P1	USB P2	USB P3	USB P4	USB P5	USB P6
H510	U3.2 Gen1x1	U3.2 Gen1x1	U3.2 Gen1x1	U3.2 Gen1x1	NA	NA
B560	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen1x1	U3.2 Gen1x1
H570	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen1x1	U3.2 Gen1x1
Z590	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
Q570	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
W580	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
	Gen2x2		Gen2x2		Gen2x2	

Intel 500 series PCH USB20 configuration						
ITEM	USB P1~9	USB P10	USB P11	USB P12	USB P13	USB P14
H510	USB2	NA	NA	NA	NA	For Intel® Wireless AC
B560	USB2	USB2	USB2	NA	NA	
H570	USB2	USB2	USB2	USB2	USB2	
Z590	USB2	USB2	USB2	USB2	USB2	
Q570	USB2	USB2	USB2	USB2	USB2	
W580	USB2	USB2	USB2	USB2	USB2	

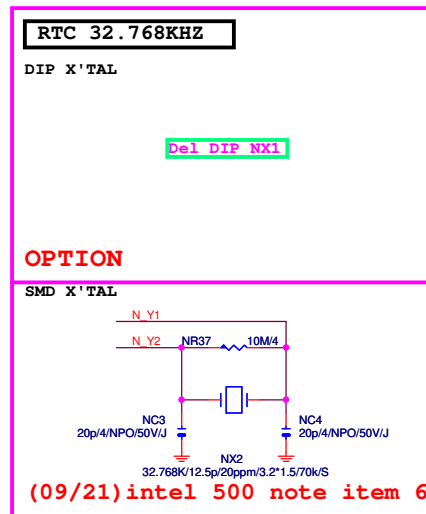


RKL_TGP_PCH-H R0.1



Intel 500 series PCH PCIE P5~P12							
ITEM	PCIE P5	PCIE P6	PCIE P7	PCIE P8	PCIE P9	PCIE P10	PCIE P11
H510	PCIE /Gbe	PCIE	PCIE	PCIE	Gbe ONLY	N/A	PCIE
B560	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE SATA_0'	PCIE SATA_1' Gbe
H570	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE SATA_0'	PCIE SATA_1' Gbe
Z590	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE SATA_0'	PCIE SATA_1' Gbe
Q570	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE SATA_0'	PCIE SATA_1' Gbe
W580	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE SATA_0'	PCIE SATA_1' Gbe
Intel® RST for x2/x4 M.2							

Intel 500 series PCH PCIE P13~P24											
ITEM	PCIE P13	PCIE P14	PCIE P15	PCIE P16	PCIE P17	PCIE P18	PCIE P19	PCIE P20	PCIE P21	PCIE P22	PCIE P23
H510	SATA_0 /Gbe	SATA_1	SATA_2	SATA_3	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B560	SATA_0 /Gbe	SATA_1	SATA_2	SATA_3	SATA_4	SATA_5	N/A	N/A	PCIE	PCIE	PCIE
H570	PCIE SATA_0 Gbe	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE
Z590	PCIE SATA_0 Gbe	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE
Q570	PCIE SATA_0 Gbe	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE
W580	PCIE SATA_0 Gbe	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE SATA_6	PCIE SATA_7	PCIE	PCIE	PCIE
Intel® RST for x2/x4 M.2						Intel® RST for x2/x4 M.2					



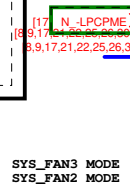
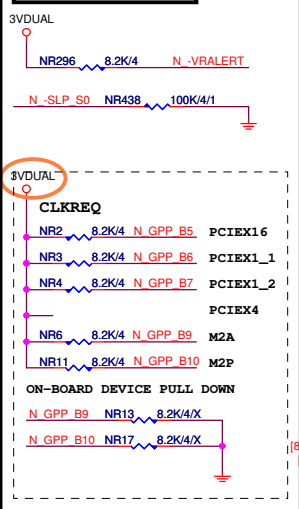
Intel 500 series PCH USB P7~P10				
ITEM	USB P7	USB P8	USB P9	USB P10
H510	NA	NA	NA	NA
B560	NA	NA	NA	NA
H570	U3.2 Gen1x1	U3.2 Gen1x1	PCIE	PCIE
Z590	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
Q570	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen1x1	U3.2 Gen1x1
W580	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1

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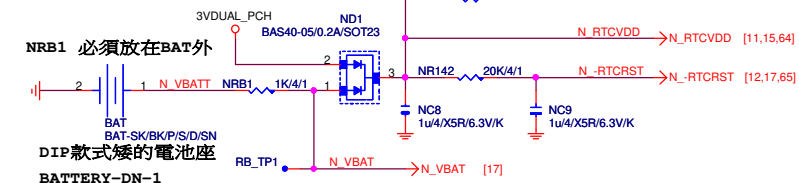
ANS	8594505	Gigabyte Technology
Title	PCH PCIE,SATA	
Size Custom	Document Number	B560M DS3H
Date:	Friday, January 22, 2021	Sheet 12 of 72

GPP_D	PU/PD
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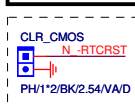
GPP_B PU/PD



BATTERY



CLR_CMOS



PCH Signal Glitch Free



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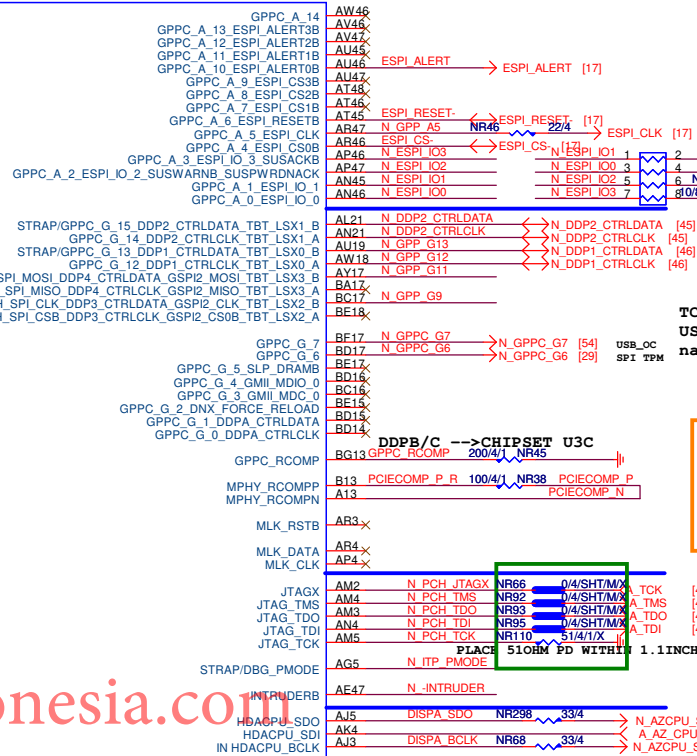
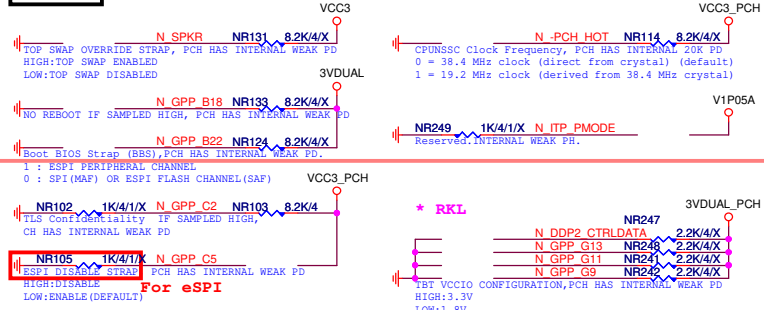
GPP_D_23 UART3_CTSB_THC1_SPI2_INTB
GPP_D_22 UART3_RTSB_THC1_SPI2_RSTB
GPP_D_21 UART3_TXD_THC1_SPI2_IO_3
GPP_D_20 UART3_RXD_THC1_SPI2_IO_2
GPP_D_19 GSPB_MOSI_THC1_SPI2_IO_1
GPP_D_18 GSPB_MISO_THC1_SPI2_IO_0
GPP_D_17 GSPB_CLK_THC1_SPI2_CLK
GPP_D_16 GSPB_CS0B_THC1_SPI2_CS0B
GPP_D_15 SML1DATA
GPP_D_14 SPI1_IO_3_THC0_SPI1_IO_3
GPP_D_13 SPI1_IO_2_THC0_SPI1_IO_2
GPP_D_12 ISH_UART0_CTSB_SML0BALERTB
GPP_D_11
GPP_D_10 SML0DATA
GPP_D_9 SML0CLK
GPP_D_8 I2S2_SCLK_THC0_SPI1_INTB
GPP_D_7 I2S2_RXD_THC0_SPI1_RSTB
GPP_D_6 I2S2_TXD_THC0M_CLKREQ_CRF_XTAL_CLKREQ
GPP_D_5 I2S2_CLK_THC0M_CNV_RF_RESET_B
GPP_D_4 SML1CLK
GPP_D_3 SPI1_MOSI_IO_0_THC0_SPI1_IO_0_SBK_3_BK5P
GPP_D_2 SPI1_MISO_IO_1_THC0_SPI1_IO_1_SBK_2_BK_2
GPP_D_1 SPI1_CLK_THC0_SPI1_CLK_SBK_1_BK_1
GPP_D_0 SPI1_CS0B_THC0_SPI1_CS0B_SBK_0_BK_0

GPP_C_23 UART2_CTSB_CNV_MFUARTO_CTS_B
GPP_C_22 UART2_RTSB_CNV_MFUARTO_RTS_B
GPP_C_21 UART2_TXD_CNV_MFUARTO_TXD
GPP_C_20 UART2_RXD_CNV_MFUARTO_RXD
GPP_C_19 I2C1_SCL
GPP_C_18 I2C1_SDA
GPP_C_17 I2C0_SCL
GPP_C_16 I2C0_SDA
GPP_C_15 UART1_CTSB_ISH_UART1_CTSB
GPP_C_14 UART1_RTSB_ISH_UART1_RTSB
GPP_C_13 UART1_TXD_ISH_UART1_TXD
GPP_C_12 UART1_RXD_ISH_UART1_RXD
GPP_C_11 UART0_CTSB
GPP_C_10 UART0_RTSB
GPP_C_9 UART0_TXD
GPP_C_8 I2C2_SCL
GPP_C_7 I2C2_SDA_I2C3_SCL
GPP_C_6 I2C1_I2C2_SCL_SDA_SBK_4_BK_4
GPP_C_5 SML0ALERTB/STRAP
GPP_C_4 I2C1_UART0_TXD_SML0BCLK_I2C2_SCL
GPP_C_3 I2C1_UART0_RXD_SML0BDATA_I2C2_SDA
GPP_C_2 SMBALERTB/STRAP
GPP_C_1 SMBDATA
GPP_C_0 SMBCLK

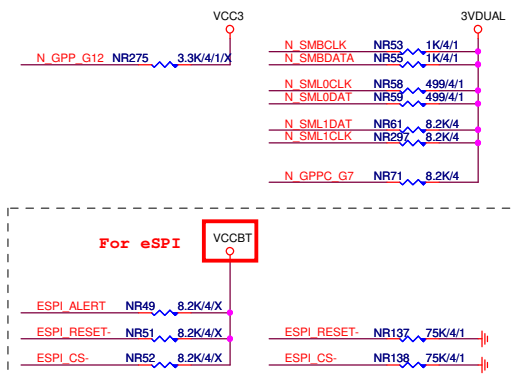
GPP_B_23 SML1ALERTB_PCHHOTB/STRAP
GPP_B_22 GSPB_MOSI
GPP_B_21 GSPB_MISO_NFC_CLKREQ
GPP_B_20 GSPB_CLK_NFC_CLKREQ
GPP_B_19 GSPB_CS0B
GPP_B_18 GSPB_MOSI/STRAP
GPP_B_17 GSPB_MISO
GPP_B_16 GSPB_CLK
GPP_B_15 GSPB_CS0B
GPP_B_14 SPIKSTRAP
GPP_B_13 PLTRSTB
GPP_B_12 SLP_S0B
GPP_B_11 I2S1_MCLK
GPP_B_10 SR0CLKREQB_5
GPP_B_9 SR0CLKREQB_4
GPP_B_8 SR0CLKREQB_3
GPP_B_7 SR0CLKREQB_2
GPP_B_6 SR0CLKREQB_1
GPP_B_5 SR0CLKREQB_0
GPP_B_4 CPU_GP_3
GPP_B_3 CPU_GP_2
GPP_B_2 VRALEB
GPP_B_1 GSPB1_CS1B_TIME_SYNC_1
GPP_B_0 GSPB0_CS1B

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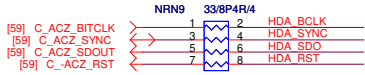
STRAP



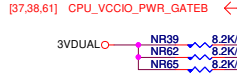
GPPC_A/GPPC_G (VCCPRIM_3P3 or VCCPRIM_1P8):
each pin voltage is selected by setting the
corresponding voltage select soft strap of the pin.



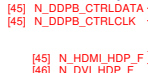
RKL_TGP_PCH-H R0.1



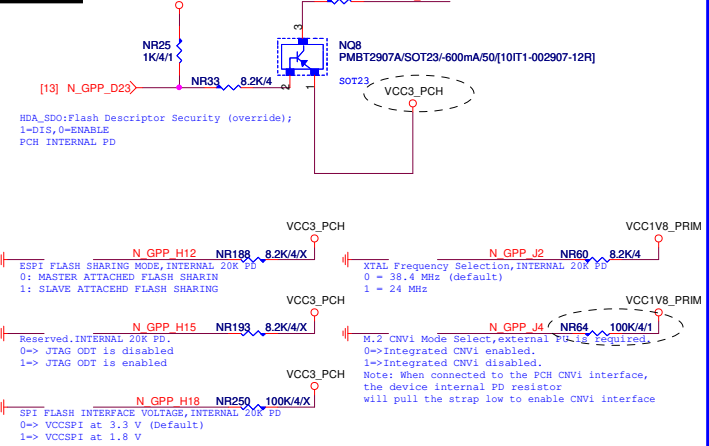
CNVI WIFI/BT DISABLE
PCIEX8 PRESENT
M2P_CPU DETECT



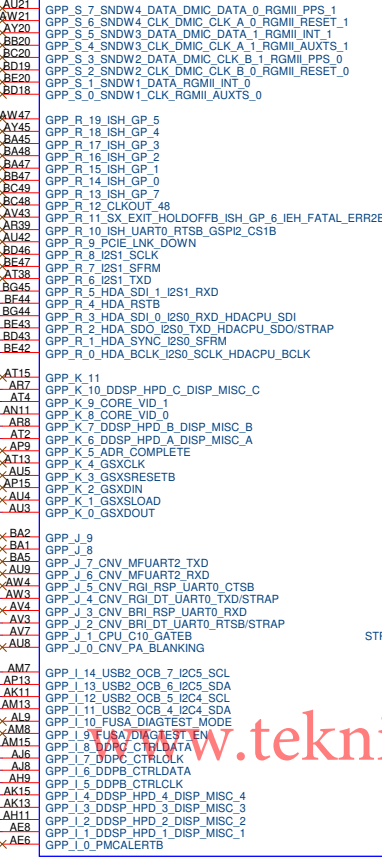
DDPA -->CHIPSET U3D



STRAP



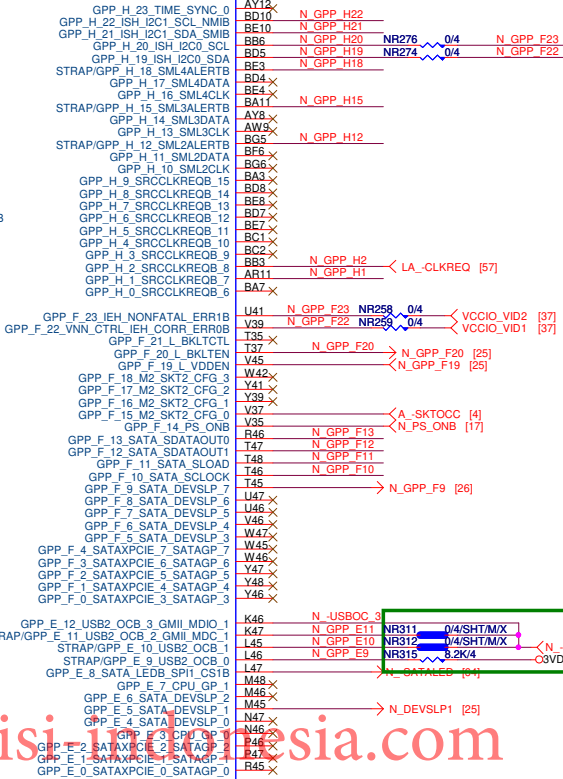
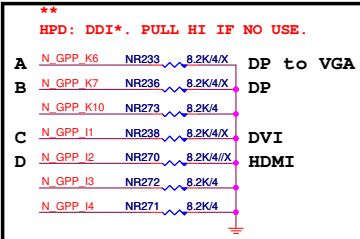
PCHC



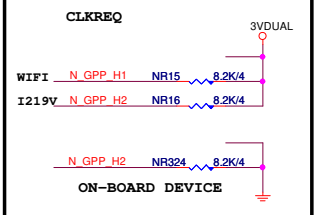
FH82B560 SRKM5/S

Fixed voltage on certain GPIO groups: GPD (3.3 V), GPP_J and GPP_S (1.8 V/VCCPRIM_1P8)

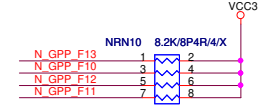
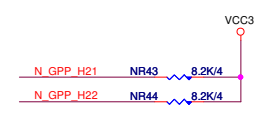
Display Port DDC/HOT PLUG SIGNAL		
CPU PORT	PCH DDC	PCH HPD
DDI_A/EDP	GPP_G0/G1	GPP_K6
DDI_1/B	GPP_I5/I6	GPP_K7
DDI_2/C	GPP_G12/G13	GPP_I1
DDI_3/D	GPP_G14/G15	GPP_I2



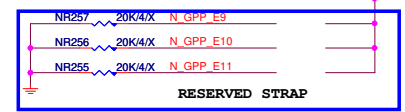
VCCIO VID
M2A_PCH IFDET
M2A_PCH DETECT



注意:PWM SIDE PD 100K. 3VDUAL



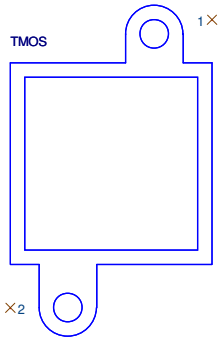
Internal pullup



ANS 8594505		Gigabyte Technology	
Title			
PCH GPP,HDA			
Size	Document Number		Rev
Custom	B560M DS3H		1.0
Date:	Friday, January 22, 2021	Sheet	14 of 72

裝甲HEATSINK 分成四大部份

MOS_HS

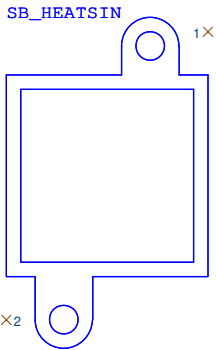


SAME Z390 UD Thermal

HEAT SINK/[12SP2-S09426-G1R_12SP2-S09426-G2R_12SP2-S09426-G3R]X

Footprint :
MOSHSINK-Z370_HD3P-T
PN: 12SP2-S09426-41R/42R/43R

PCH_HS



SAME B460M D3H Thermal

PCH_HS
PCH HS/BLACK/UD LOGO/KG/[12SP2-S04207-K1R_12SP2-S04207-K2R_12SP2-S04207-K3R]

FOOTPRINTS :
sink_b550m_aorus_pro_pch

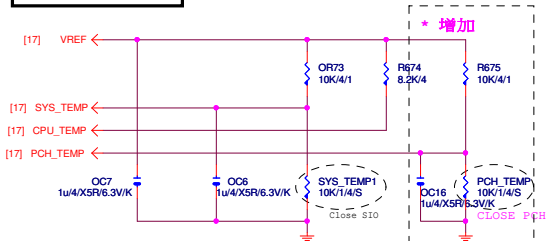
裝甲

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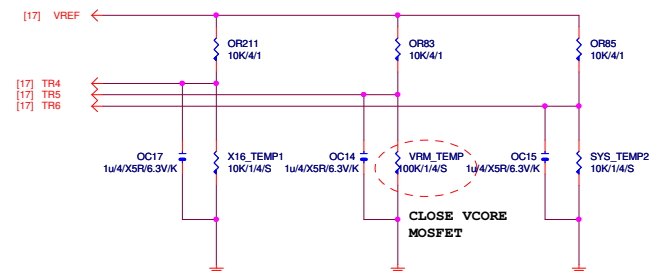
後窗鐵片

- * PCB顏色 : 咖啡黑
- * 文字面 : 灰色
- * 疊構 : B

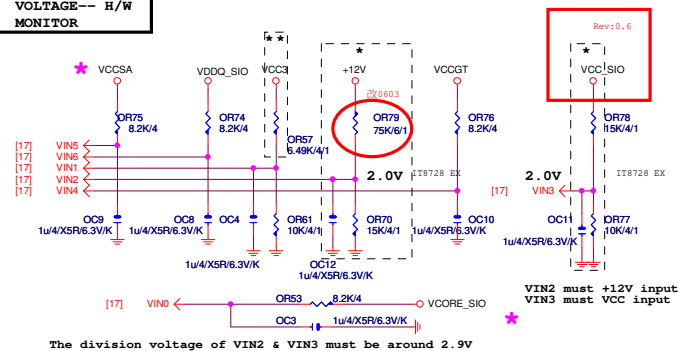
TEMP H/W MONITOR



5個FAN時使用



VOLTAGE-- H/W MONITOR



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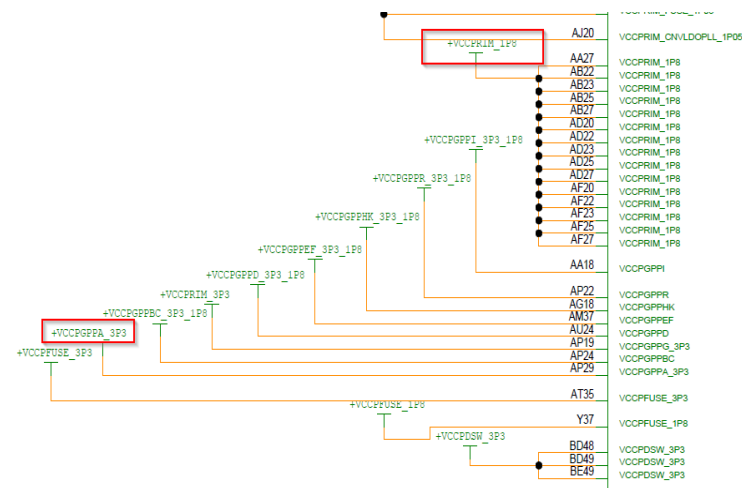
JP4 HI ESPI MODE VCCBT 3.3V

JP5 HI ESPI MODE LPC I/F

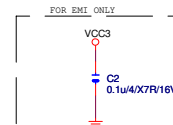
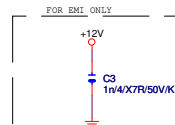
JP4 LO ESPI MODE VCCBT 1.8V

JP5 LO ESPI MODE ESPI I/F

VCCBT PWF R9 06/X 03VDUAL
VCCBT PWF R10 06 0VCC1V8_PRIM
For eSPI



(靠近ATX CONNECTOR)

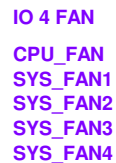


★Update 2015-04.24

Gigabyte Technology

Title	HWM,KB/MS, FAN CTRL		
Size	Document Number	B560M DS3H	Rev 1.0
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CPU FAN

[illegible]

SYSTEM FAN2

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VCC3

FBR1 1K/4/1

FBR2 100K/4/1

[17] FANPWM3

FBC3 10u/8/X5R/16V/K

+12V

FAN2DCIN

FAN2_MODE

FBC1 0.1u/4/X7R/16V/K

[13] N_GPP_B15

FBR6 0/4/SHT/10M/X

**MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.**

FBDU1

VIN

PWMOUT

VOUT

2 FAN2_PWMOUT

4 FAN2_VOUT

3 NC

7 NC

9 PGND

NCT3947SOP8-EP

FAN2_VOUT

SFAN2_3

FBR4 15K/4/1

FAN2_PWMOUT

FAN114 BK/A3/PA66

SYS_FAN2

FBC2 10u/8/X5R/16V/K

FBR5 6.2K/4/1

FANIO3 [17]

[illegible]

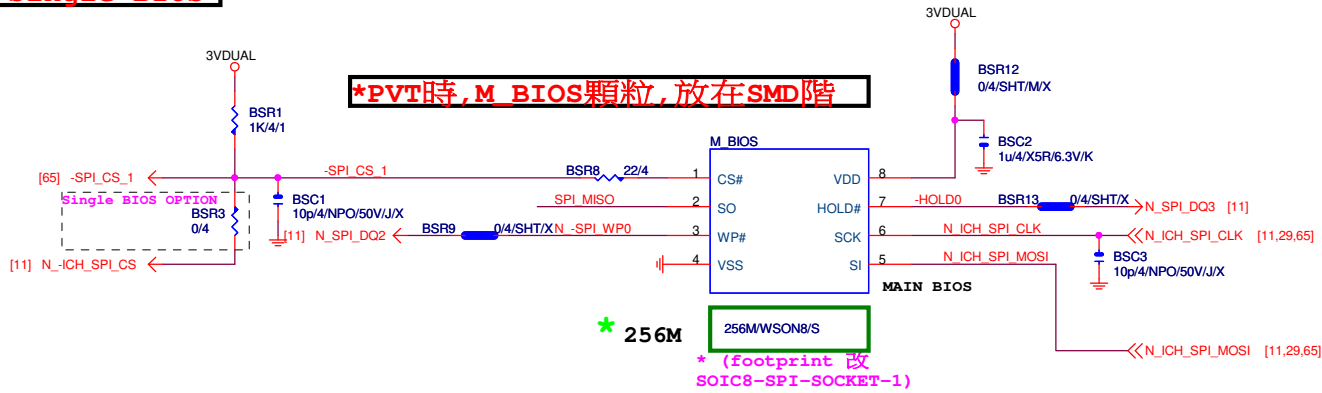
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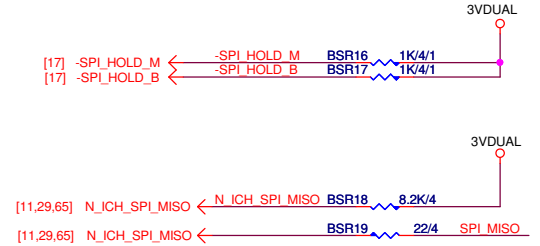
Title				HWM,KB/MS, FAN CTRL			
Size	Custom	Document Number				Rev	
		B560M DS3H				1.0	
Date:	Tuesday, December 29, 2020			Sheet	19	of	72

DUAL BIOS *Single BIOS

*PVT時, M_BIOS顆粒, 放在SMD階



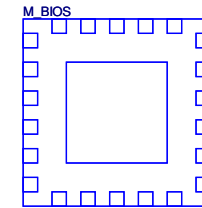
MOSI For DMI RX Termination Voltage



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K

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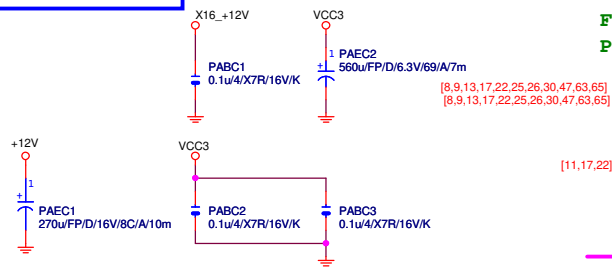
LCP/G-FL/1.27mm/200MIL/WHITE[10SL2-000008-71R]/X

* 試產先上, PVT 移除

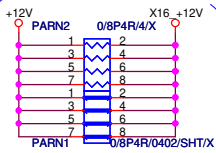
Gigabyte Technology

Title			BIOS
Size	Document Number	Rev	
Custom	B560M DS3H	1.0	
Date:	Monday, January 04, 2021	Sheet	20 of 72

PCIEX16 SLOT



PCIEX16 PROTECT SHT



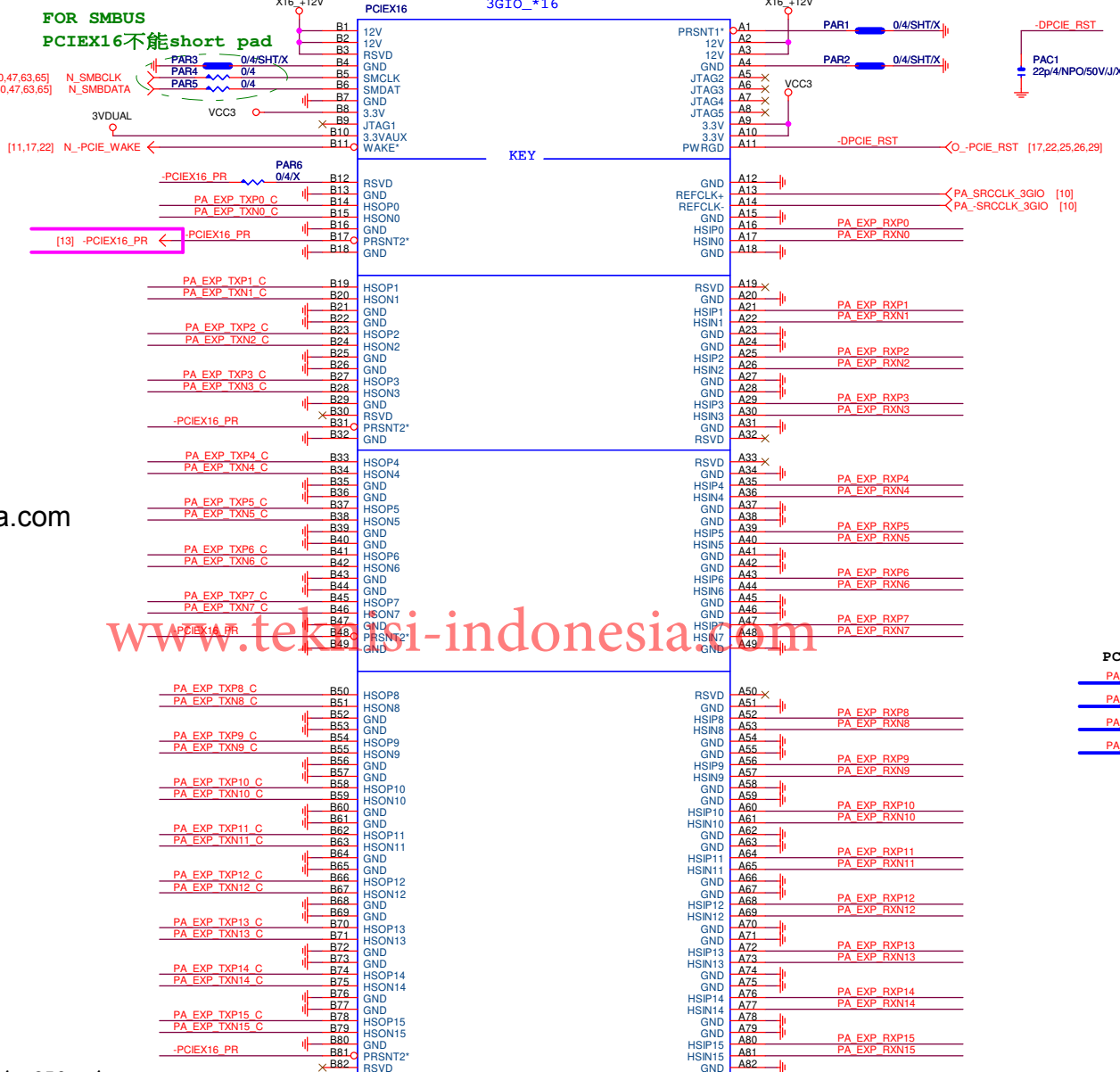
```
+12 protect
short-wire test
```

PCIEX16	AC	CAP
---------	----	-----

PA EXP TXP0	PAC5	0.22u4/4X5R6.3V/K	PA EXP TXP0_C
PA EXP TXN0	PAC4	0.22u4/4X5R6.3V/K	PA EXP TXN0_C
PA EXP TXP1	PAC6	0.22u4/4X5R6.3V/K	PA EXP TXP1_C
PA EXP TXN1	PAC7	0.22u4/4X5R6.3V/K	PA EXP TXN1_C
PA EXP TXP2	PAC8	0.22u4/4X5R6.3V/K	PA EXP TXP2_C
PA EXP TXN2	PAC9	0.22u4/4X5R6.3V/K	PA EXP TXN2_C
PA EXP TXP3	PAC10	0.22u4/4X5R6.3V/K	PA EXP TXP3_C
PA EXP TXN3	PAC11	0.22u4/4X5R6.3V/K	PA EXP TXN3_C
PA EXP TXP4	PAC12	0.22u4/4X5R6.3V/K	PA EXP TXP4_C
PA EXP TXN4	PAC13	0.22u4/4X5R6.3V/K	PA EXP TXN4_C
PA EXP TXP5	PAC14	0.22u4/4X5R6.3V/K	PA EXP TXP5_C
PA EXP TXN5	PAC15	0.22u4/4X5R6.3V/K	PA EXP TXN5_C
PA EXP TXP6	PAC16	0.22u4/4X5R6.3V/K	PA EXP TXP6_C
PA EXP TXN6	PAC17	0.22u4/4X5R6.3V/K	PA EXP TXN6_C
PA EXP TXP7	PAC18	0.22u4/4X5R6.3V/K	PA EXP TXP7_C
PA EXP TXN7	PAC19	0.22u4/4X5R6.3V/K	PA EXP TXN7_C
PA EXP TXP8	PAC21	0.22u4/4X5R6.3V/K	PA EXP TXP8_C
PA EXP TXN8	PAC20	0.22u4/4X5R6.3V/K	PA EXP TXN8_C
PA EXP TXP9	PAC22	0.22u4/4X5R6.3V/K	PA EXP TXP9_C
PA EXP TXN9	PAC23	0.22u4/4X5R6.3V/K	PA EXP TXN9_C
PA EXP TXP10	PAC24	0.22u4/4X5R6.3V/K	PA EXP TXP10_C
PA EXP TXN10	PAC25	0.22u4/4X5R6.3V/K	PA EXP TXN10_C
PA EXP TXP11	PAC26	0.22u4/4X5R6.3V/K	PA EXP TXP11_C
PA EXP TXN11	PAC27	0.22u4/4X5R6.3V/K	PA EXP TXN11_C
PA EXP TXP12	PAC28	0.22u4/4X5R6.3V/K	PA EXP TXP12_C
PA EXP TXN12	PAC29	0.22u4/4X5R6.3V/K	PA EXP TXN12_C
PA EXP TXP13	PAC30	0.22u4/4X5R6.3V/K	PA EXP TXP13_C
PA EXP TXN13	PAC31	0.22u4/4X5R6.3V/K	PA EXP TXN13_C
PA EXP TXP14	PAC32	0.22u4/4X5R6.3V/K	PA EXP TXP14_C
PA EXP TXN14	PAC33	0.22u4/4X5R6.3V/K	PA EXP TXN14_C
PA EXP TXP15	PAC34	0.22u4/4X5R6.3V/K	PA EXP TXP15_C
PA EXP TXN15	PAC35	0.22u4/4X5R6.3V/K	PA EXP TXN15_C

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PCIEX16:16/5/5/5/16

```

PA_EXP_RXP[0..15]    >> PA_EXP_RXP[0..15] [4]
PA_EXP_RXN[0..15]    >> PA_EXP_RXN[0..15] [4]
PA_EXP_TXP[0..15]    >> PA_EXP_TXP[0..15] [4]
PA_EXP_TXN[0..15]    >> PA_EXP_TXN[0..15] [4]

```

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1 (單向) BANDWIDTH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1 (雙向) BANDWIDTH=2.5GHz*(8b/10b) X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWIDTH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

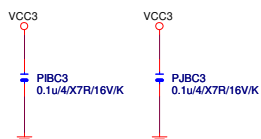
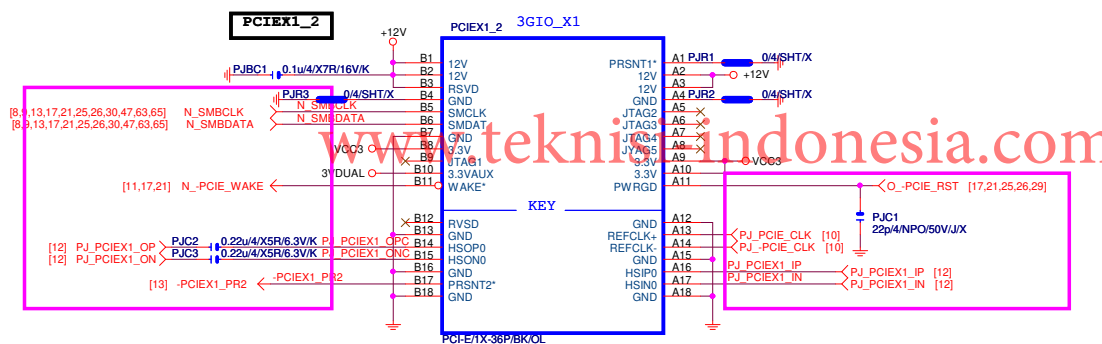
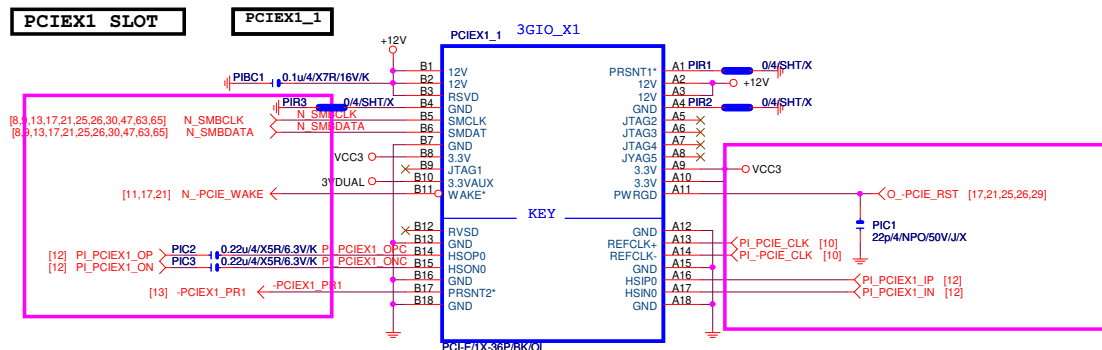
PCE-E X16 (雙向) BANDWIDTH=2.5GHz*(8b/10b)*X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

PCE-E X1 (單向) BANDWIDTH=5GHz* (8b/10b)=4Gb/s=500MB/s

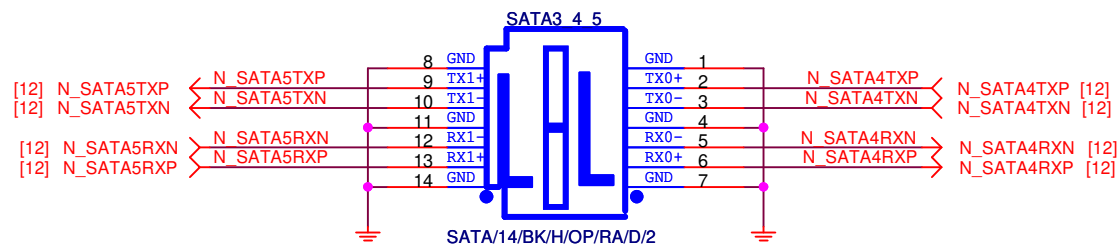
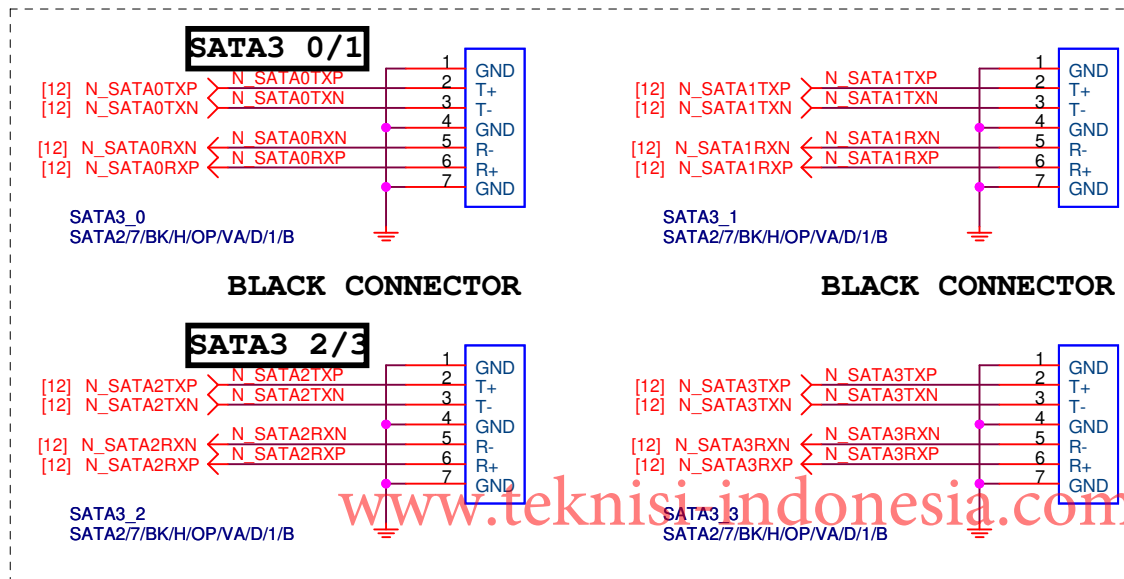
PCI-E REV:3.0--> 8GHZ

PCE-E X1 (單向) BANDWIDTH=8GHz* (128b/130b)=8Gb/s=1GB/s



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Title			
PCIE X1 *3			
Size	Document Number	Rev	
Custom	B560M DS3H	1.0	
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Rev 0.1

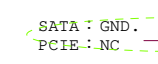
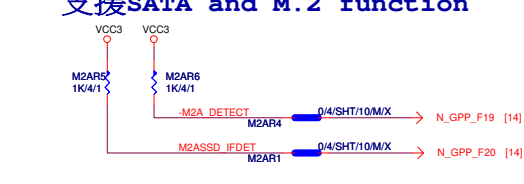
M.2 Lane4 from PCH port9

```
[12] M2_PC
M.2 Lane3 from PCH port1
[12] M2_PC
```

M.2 Lane2 from PCH port1

M.2 Lane1 from PCH port1

支援SATA and M.2 function

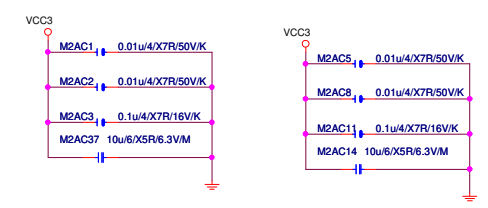
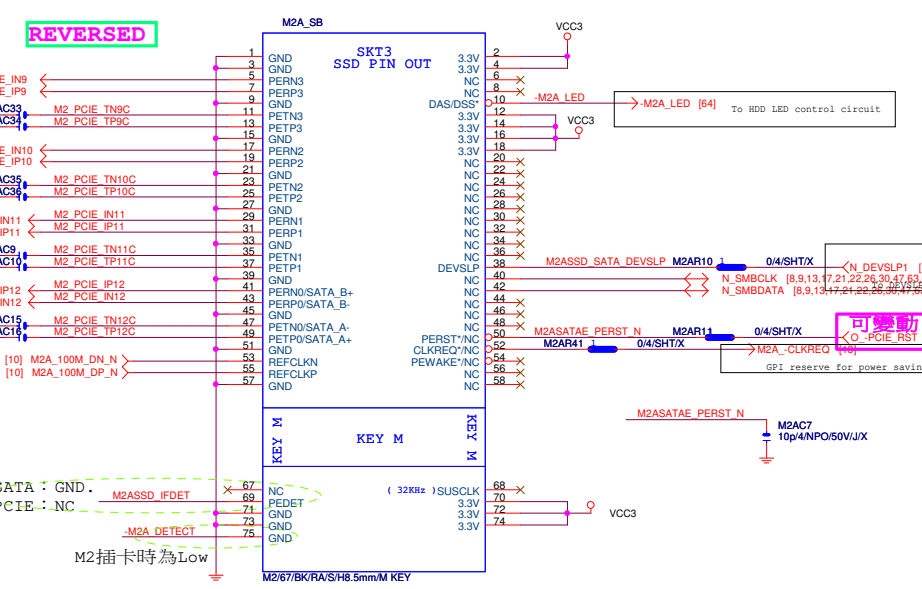


M2插卡時為Low

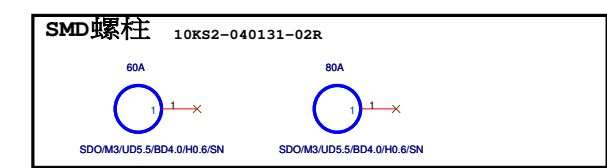
架高

Footprint : m2_80_h2mm8w

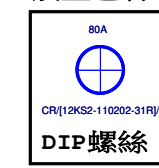
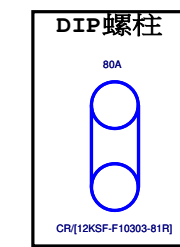
Flex IO priority	N_GPP_K1	IO14 PCIe#9	IO15 PCIe#10	IO16 PCIe#11	IO17 PCIe#12
M2A SATA	L	PCIE	PCIE	SATA 0	SATA 1
M2A PCIE (PCIE Reverse)	H	PCIE	PCIE	PCIE	PCIE



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改至包材



Rev 0.1

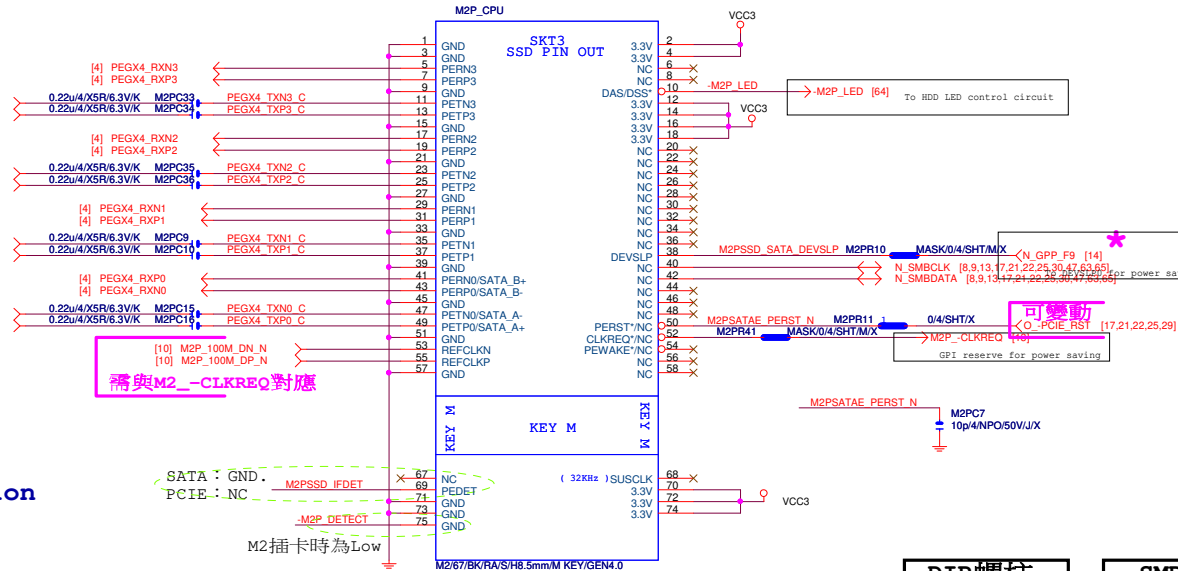
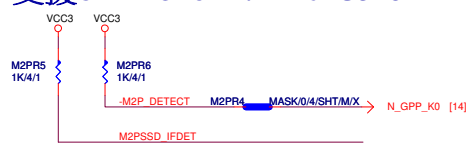
M.2 Lane4 from CPU port4

M.2 Lane3 from CPU port3

M.2 Lane2 from CPU port2

M.2 Lane1 from CPU port1

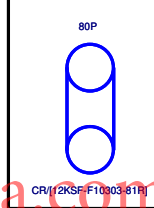
支援SATA and M.2 function



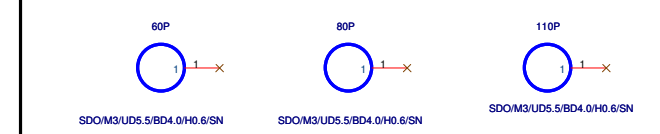
改至包材



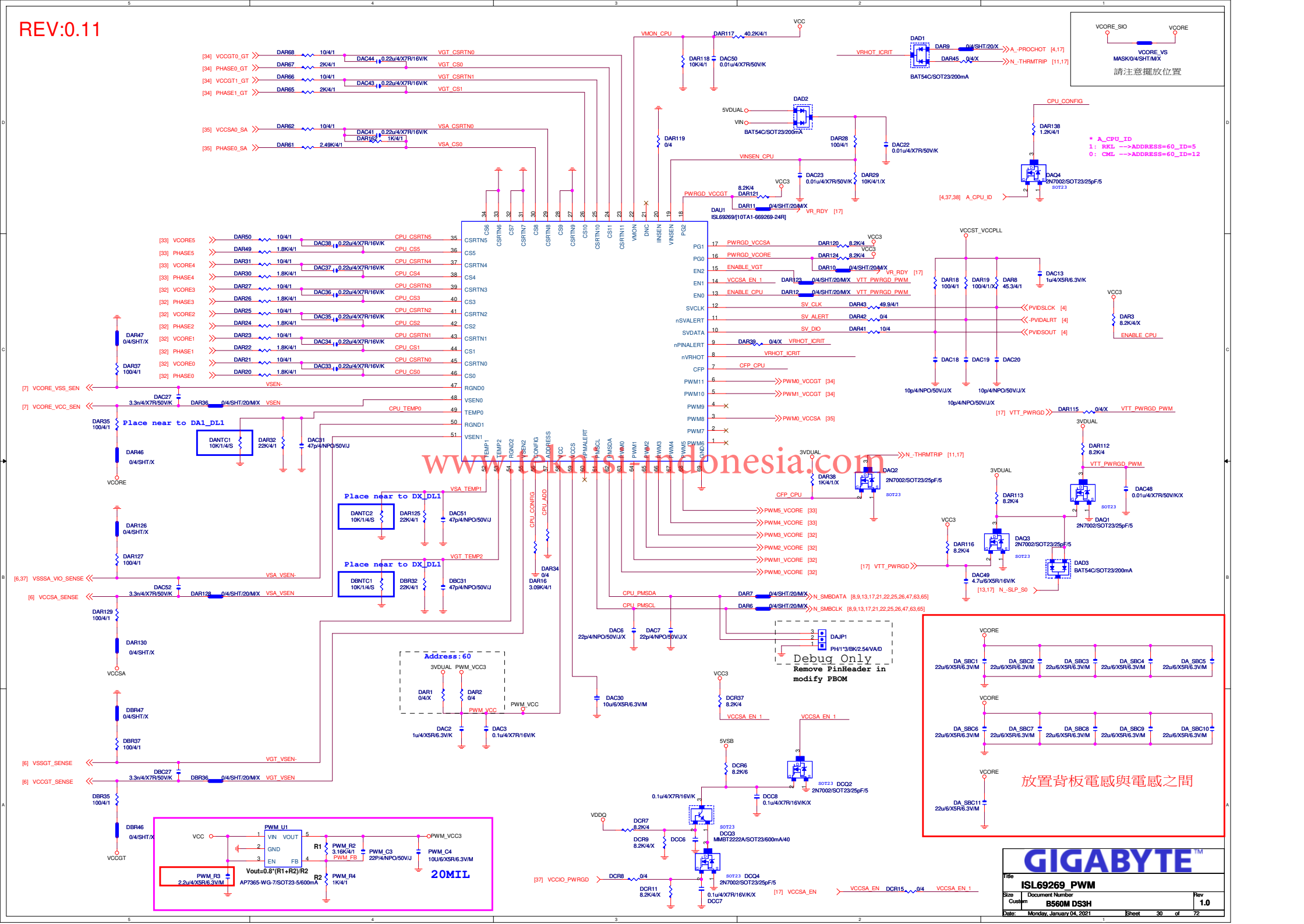
DIP螺柱

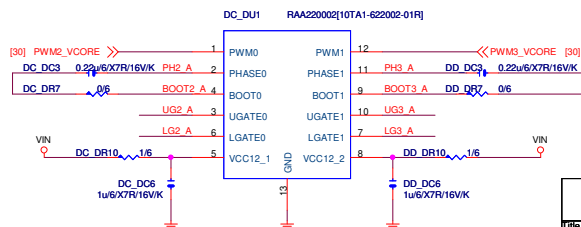
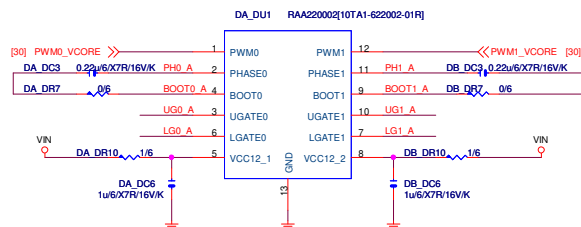
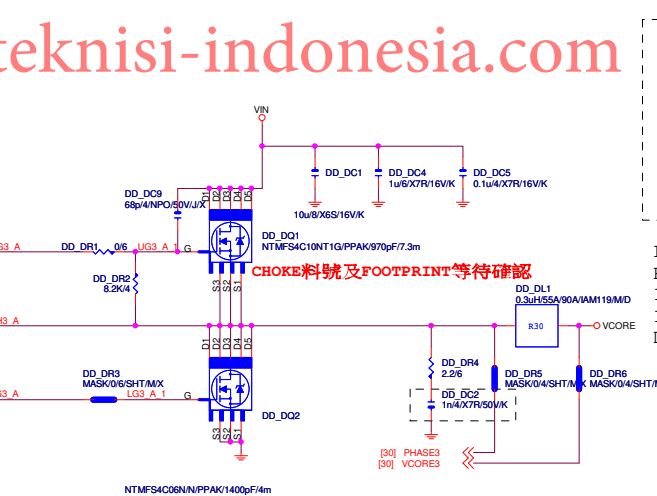
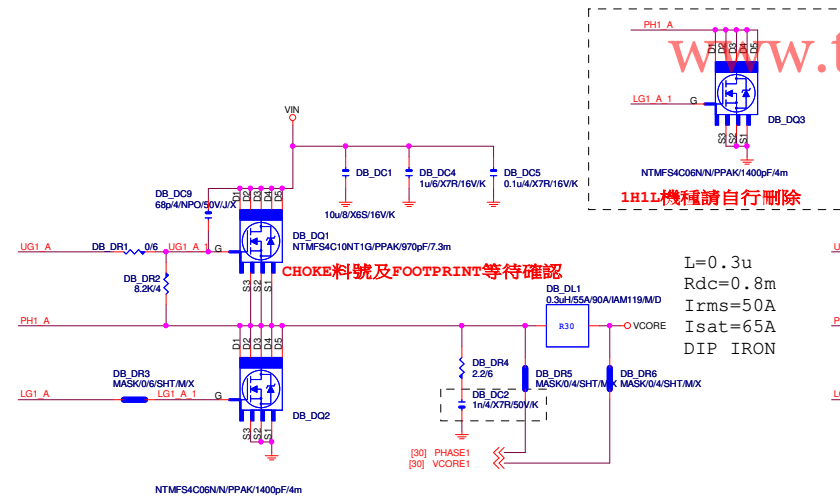
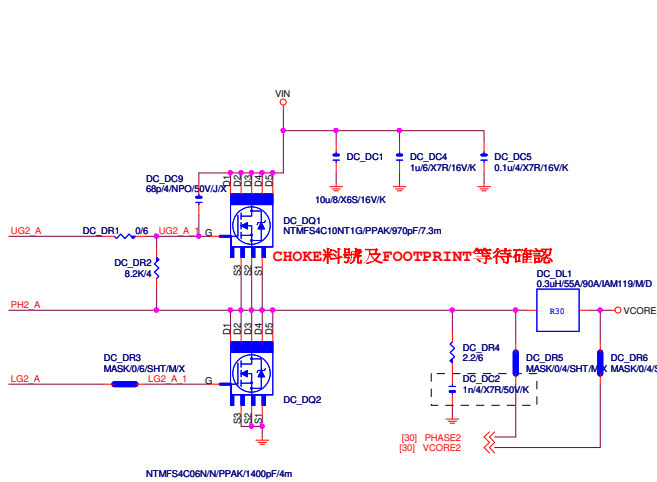
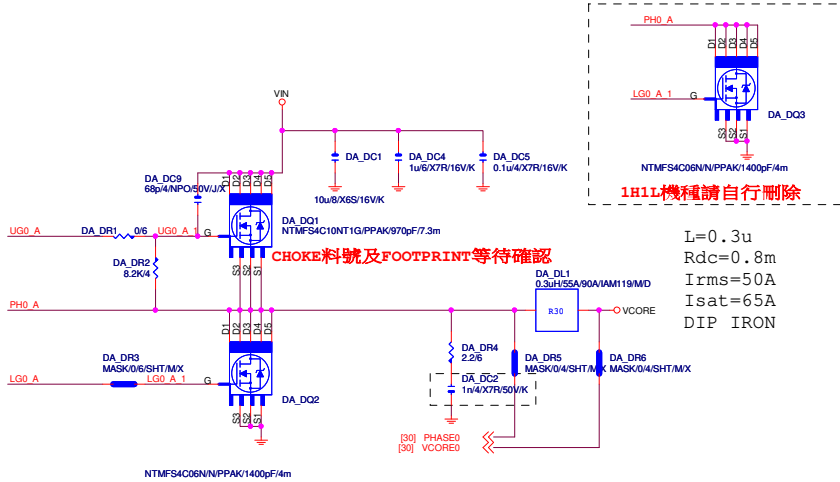


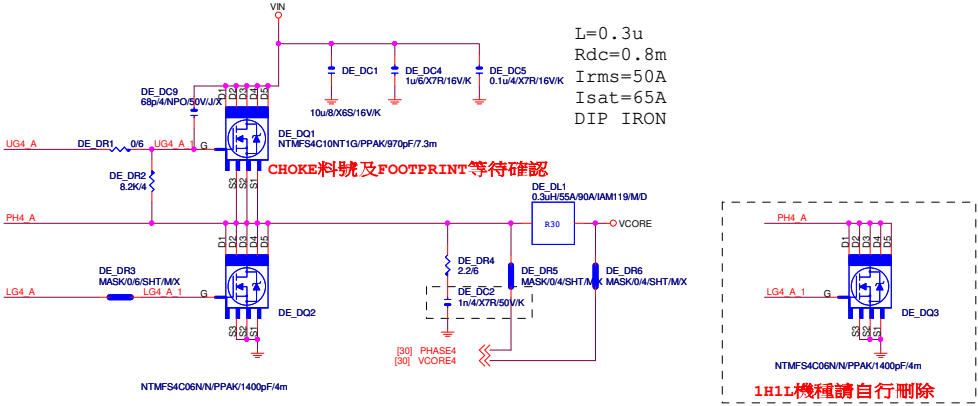
SMD螺柱



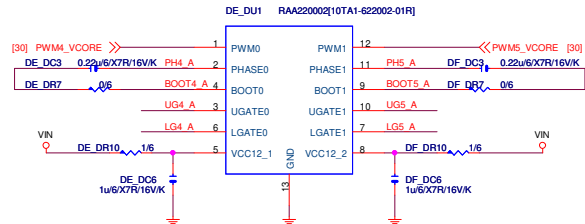
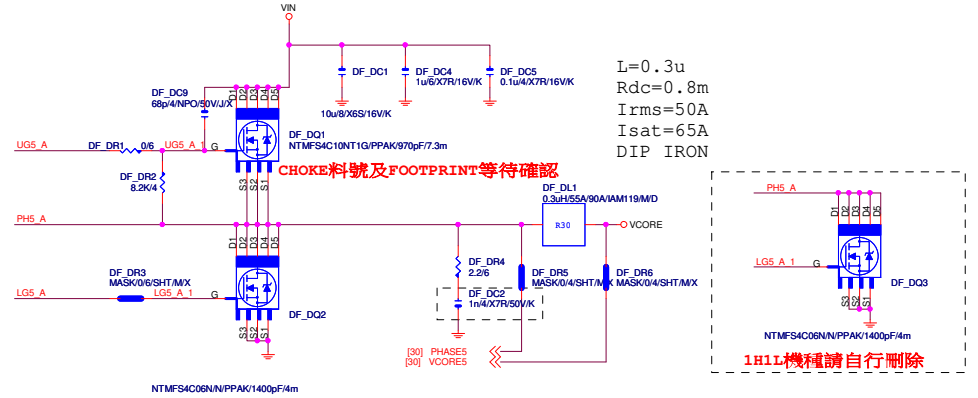
Footprint : HOLE_C236D165-A

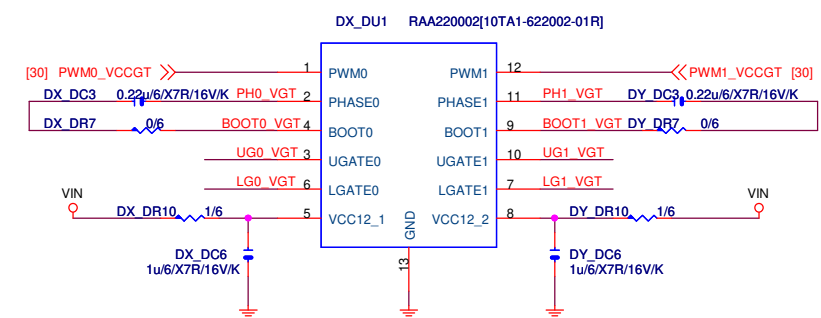
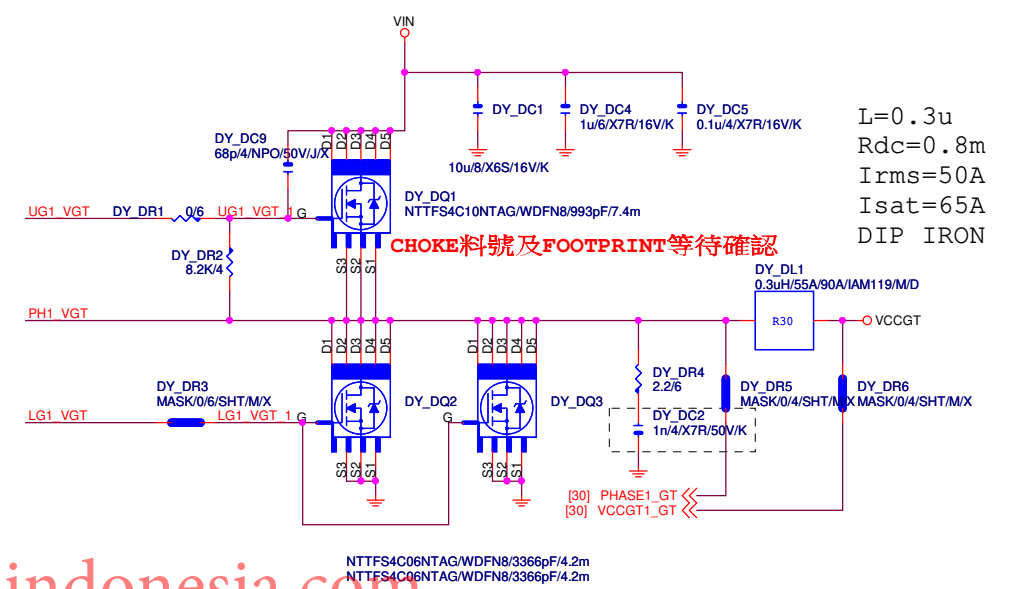
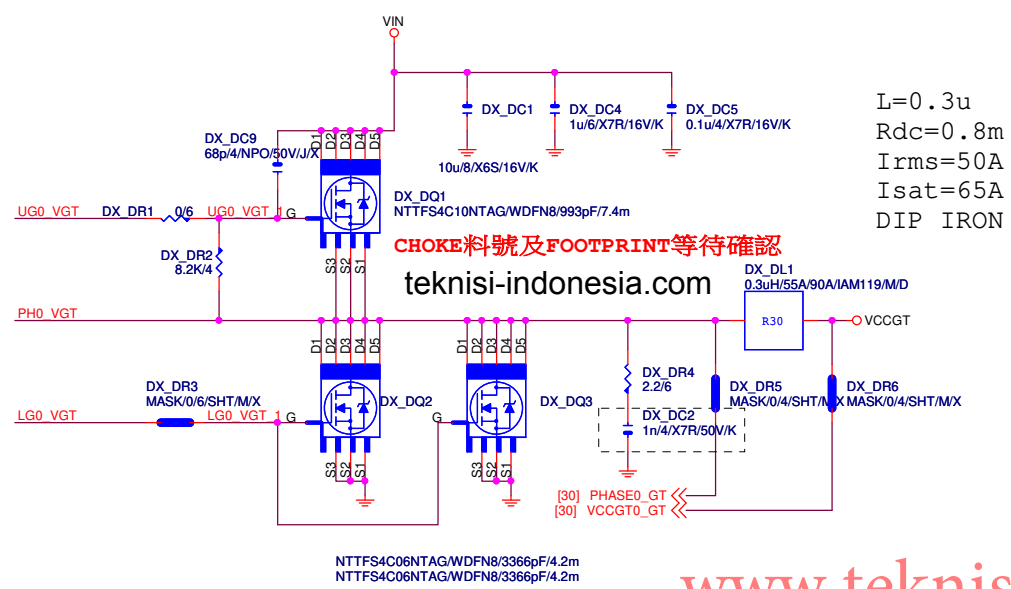






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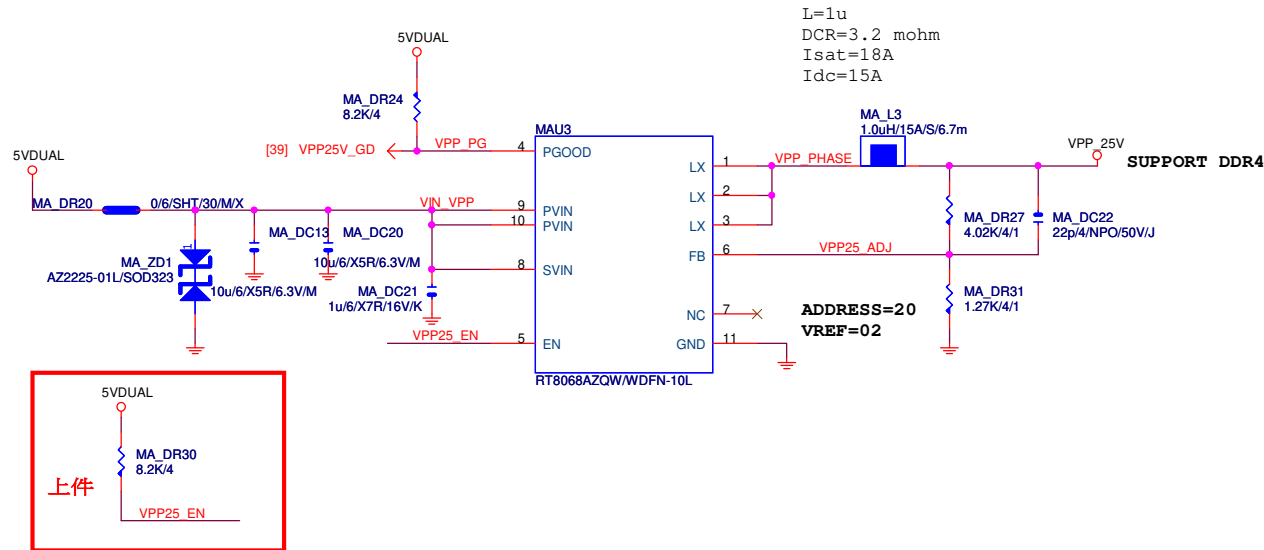
放置背板電感與電感之間

GIGABYTE™			
Title			
VCCGT_DRMOS			
Size B	Document Number		Rev 1.0
	B560M DS3H		
Date:	Tuesday, December 29, 2020	Sheet	34 of 72

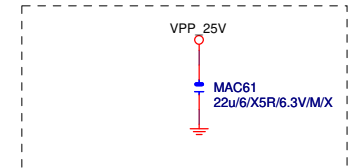
REV:0.1

VPP 25V

CHOKE與CAP料號可變



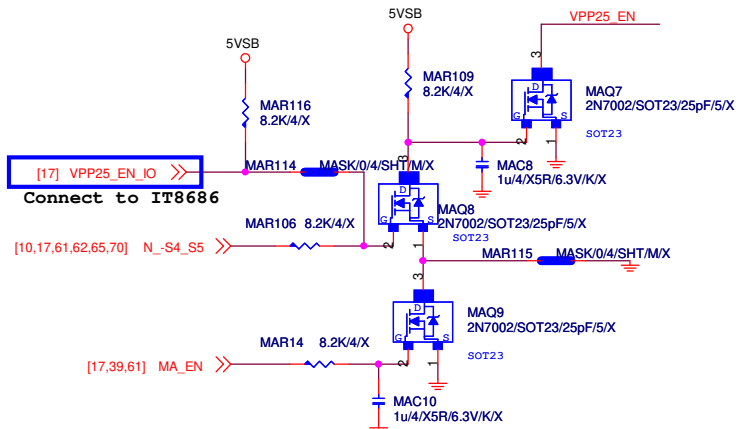
2.5V

請放置CHOKE一出來位置.先預留.
請自行確認ripple後再決定是否上件

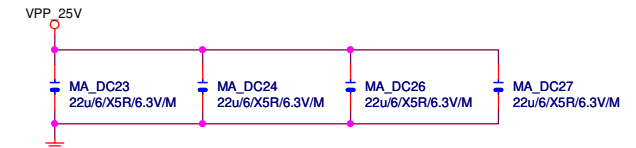
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PWR SEQ

* 刪 MA_DR32

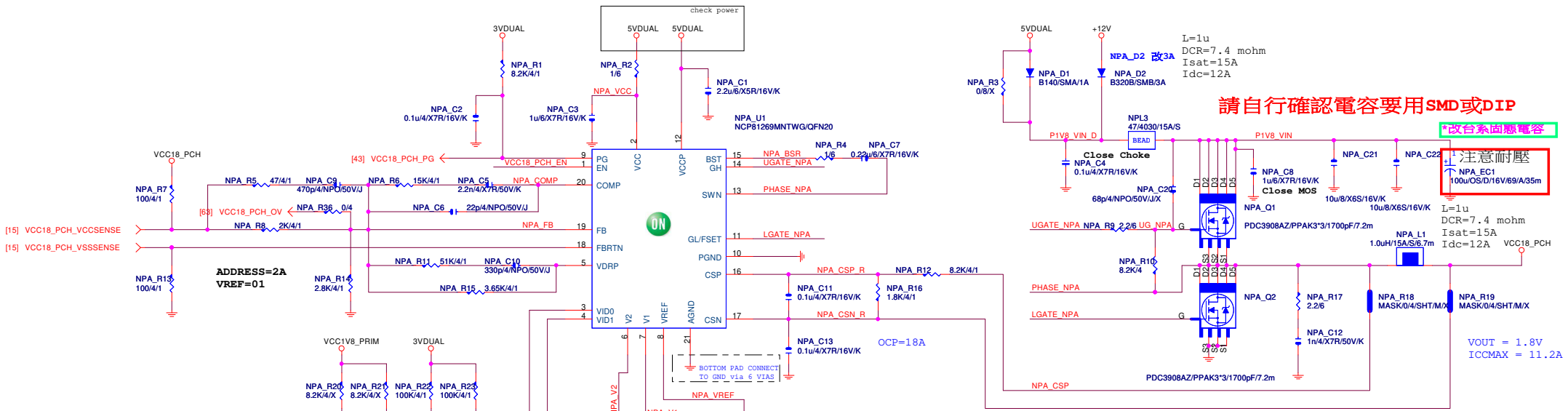


VPP CAP 22u*4PCS



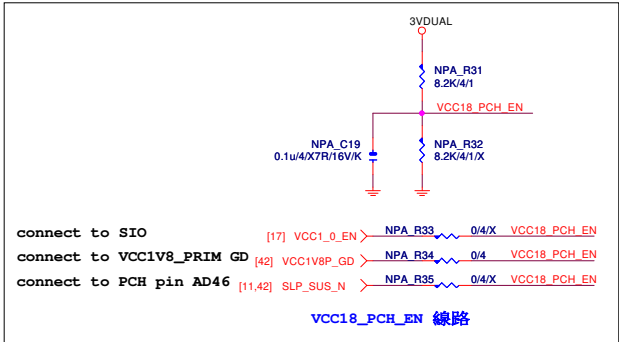
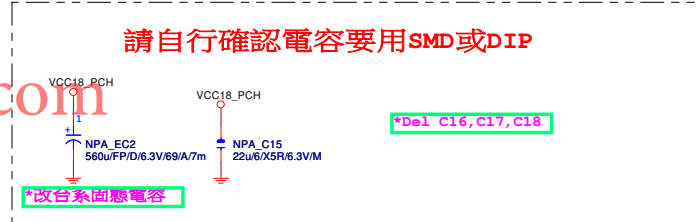
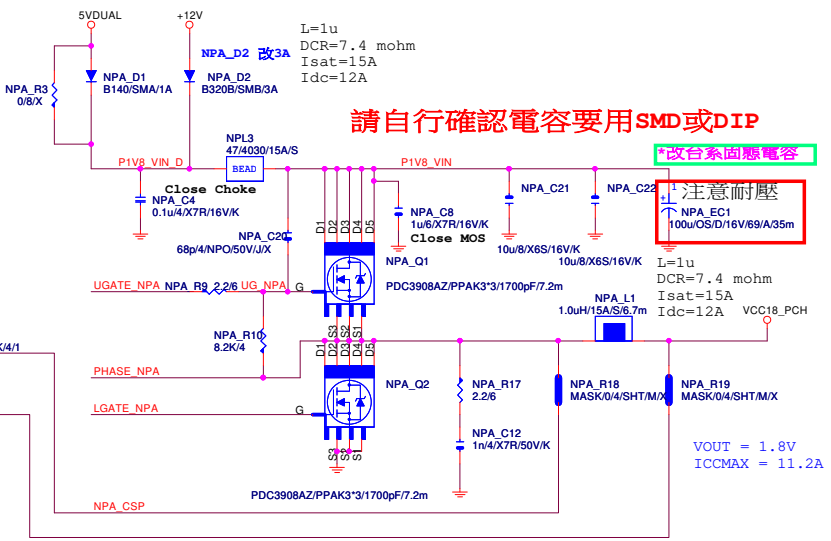
GIGABYTE™

Title		
RT8068_VPP25 POWER		
Size	Document Number	Rev
Custom	B560M DS3H	1.0
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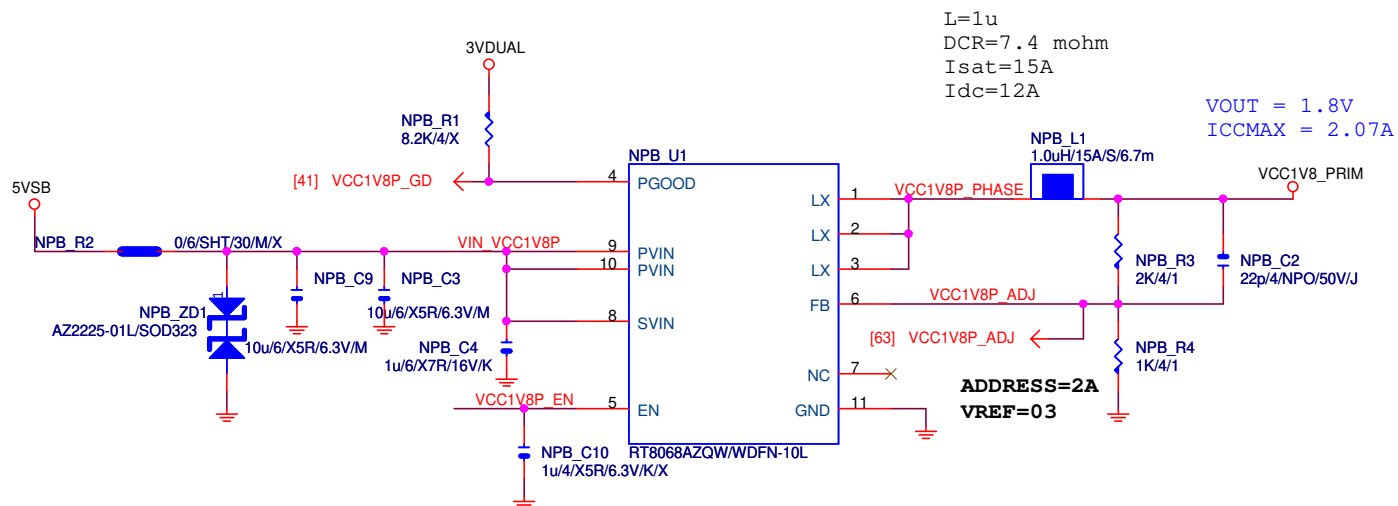
VID1	VID0	VCCIN_AUX
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

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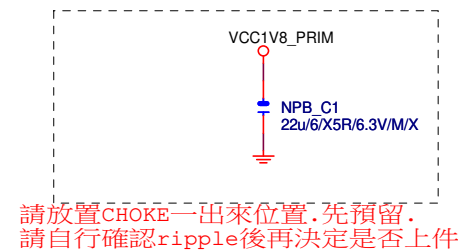


REV: 0.1

VCC1V8 PRIM

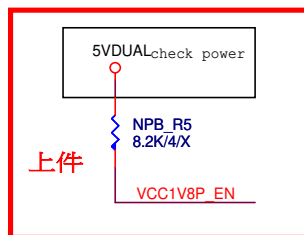


CHOKE與CAP料號可變



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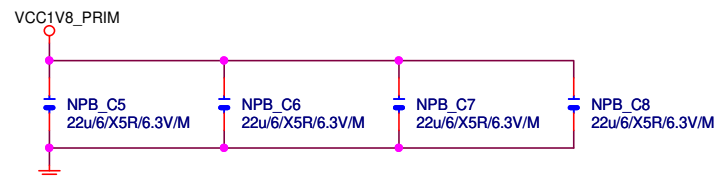
PWR SEQ



connect to PCH pin AD46

[11,41] SLP_SUS_N >> NPB_R6 0/4 VCC1V8P_EN

VCC1V8_PRIM CAP 22u*4PCS



GIGABYTE™

Title
RT8068_VCC1V8_PRIM

Size Custom Document Number
B560M DS3H

Rev
1.0

Date: Tuesday, December 29, 2020

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REV: 0.1

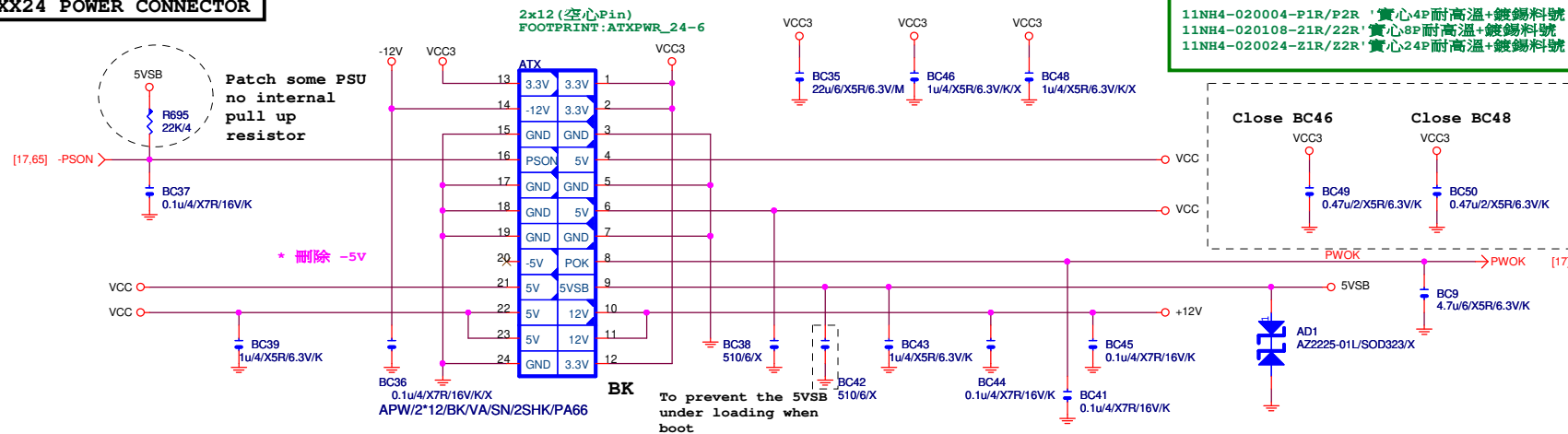
[17] 5VAUX_SW



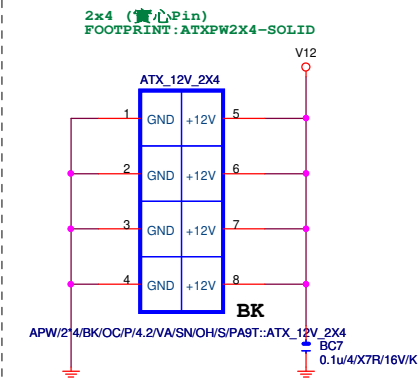
www.teknisi-indonesia.com [44] VCC18_PCH_PG >

Gigabyte Technology			
Title			
DISCRETE POWER			
Size	Document Number		Rev
Custom	B560M DS3H		1.0
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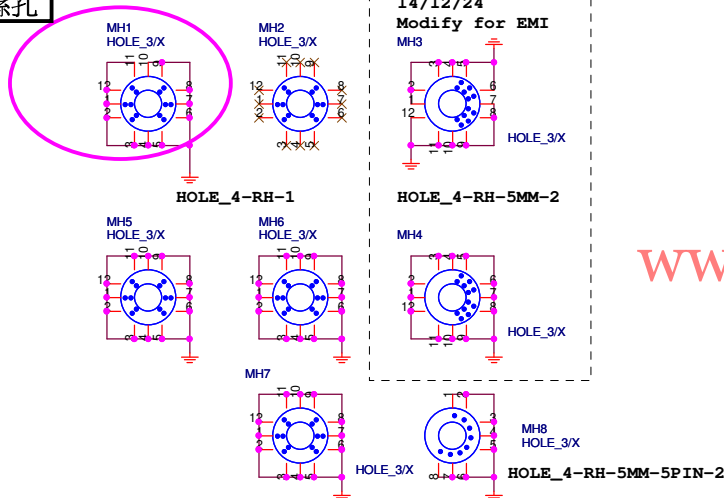
ATXX24 POWER CONNECTOR



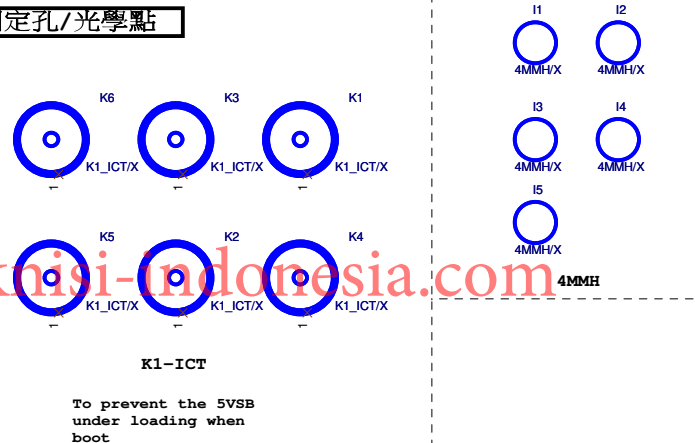
ATXX4 POWER CONNECTOR



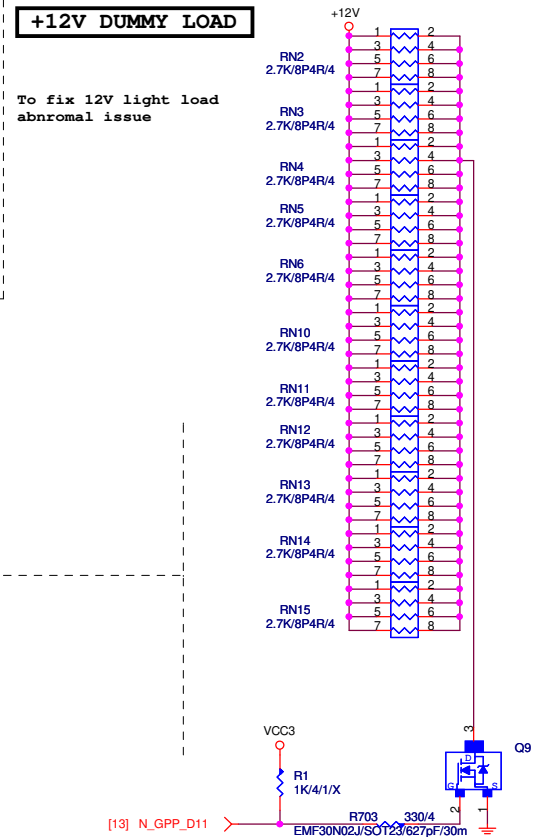
螺絲孔



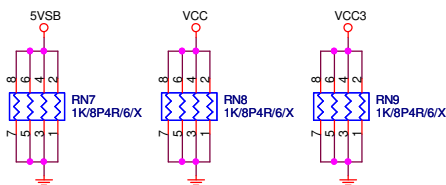
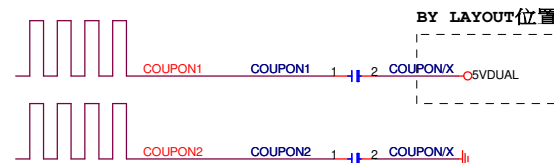
固定孔/光學點

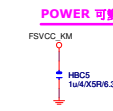


+12V DUMMY LOAD



DUMMY LOAD

**COUPON**



Display Port with HDMI, or HDMI only.

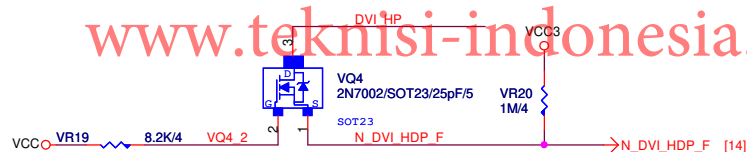
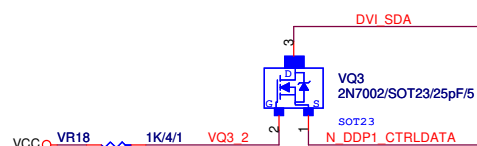
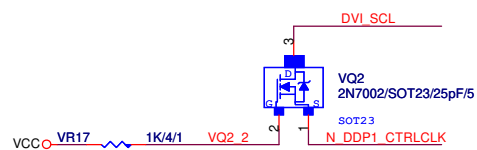
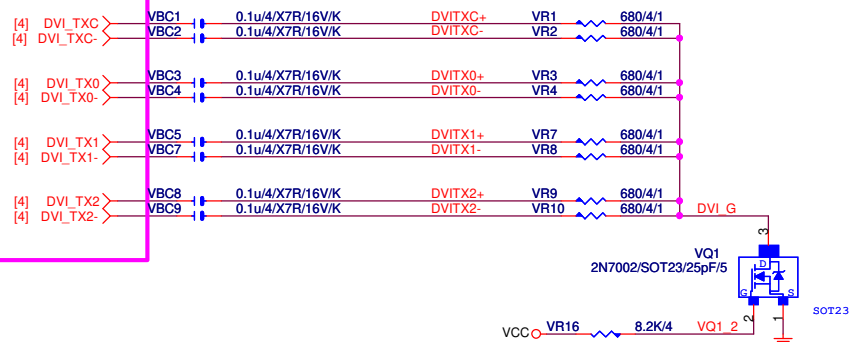


Gigabyte Technology			
Title			
HDMI_NO LS/U32			
Size	Document Number		
Custom	B560M DS3H		
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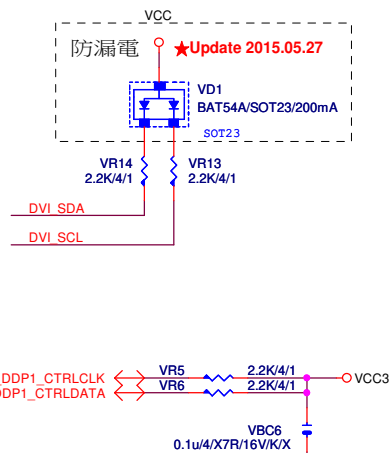
Rev: 0.8

DVI:20/4/6/4/20
Impedance=85 +- 17.5%

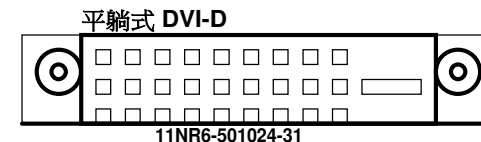
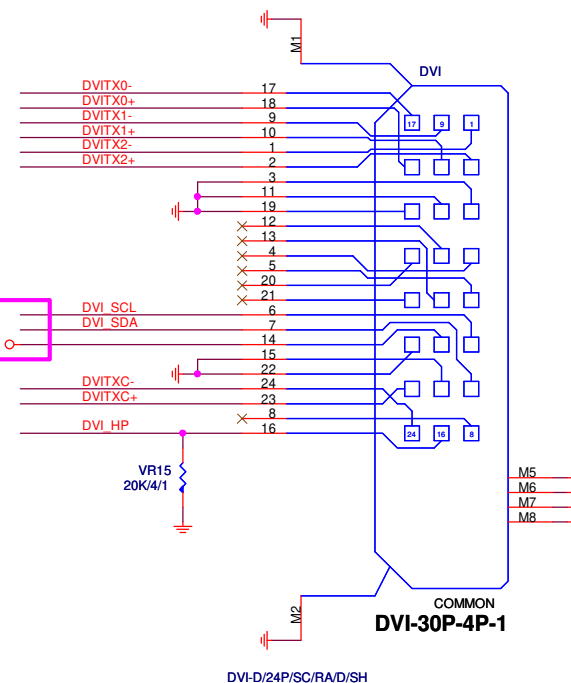
NET 可變



DVI PU

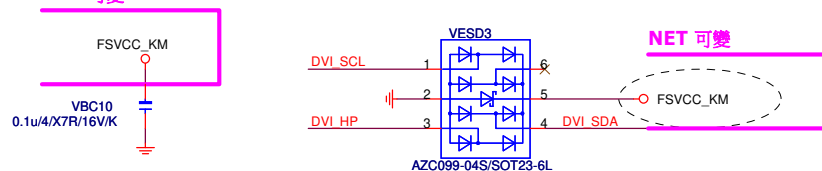


DVI CONN

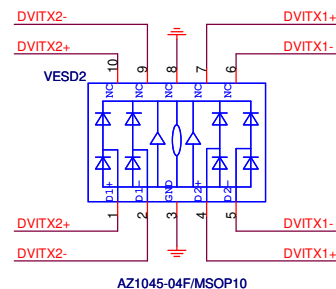


ESD

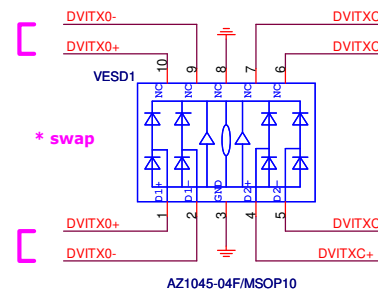
NET 可變



Close to connector



Close to connector



Close to connector

Gigabyte Technology

Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	123-129
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	78-84
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-573
5. The Effect of Catalysts on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	890-896

DVI

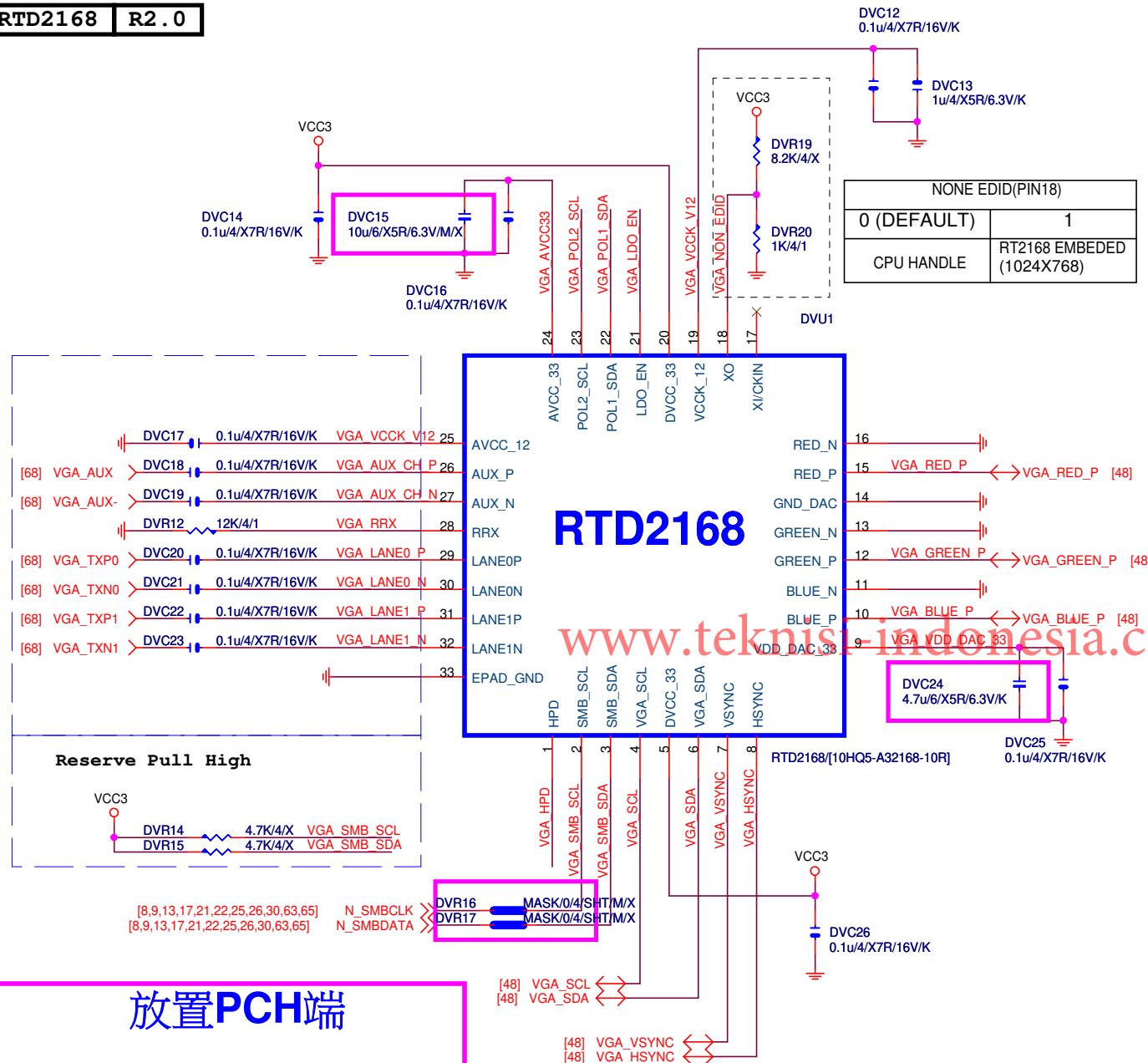
Size	
Custom	

Document Number
B560M DS3H

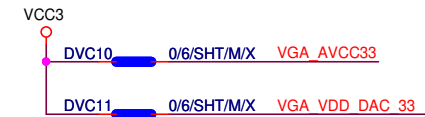
Rev	1.0
-----	-----

Date: Tuesday, December 29, 2020

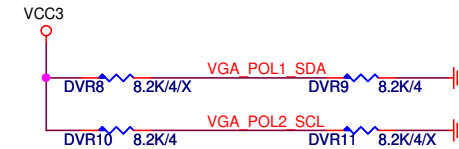
Sheet 46 of 72



POWER

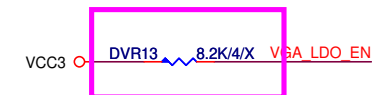


Power on latch



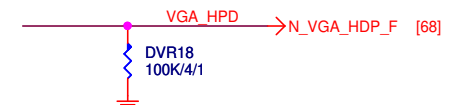
		POL1_SDA(PIN22)	
		0	1
POL2_SCL (PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

Embedded LDO

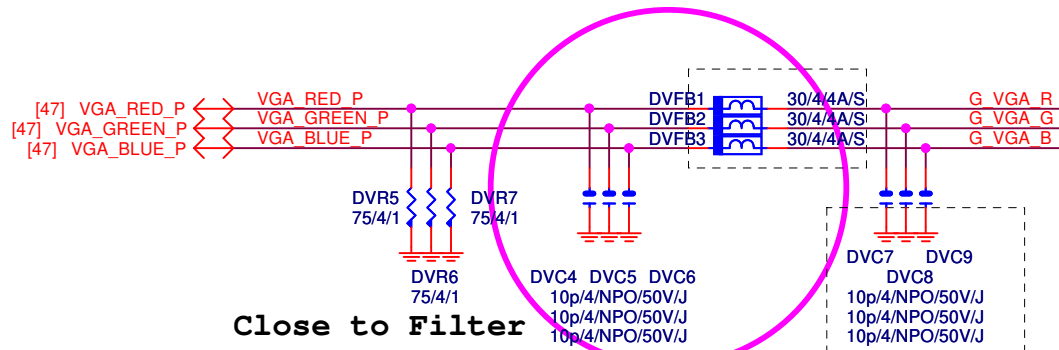
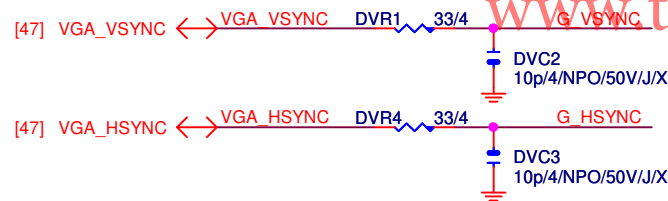
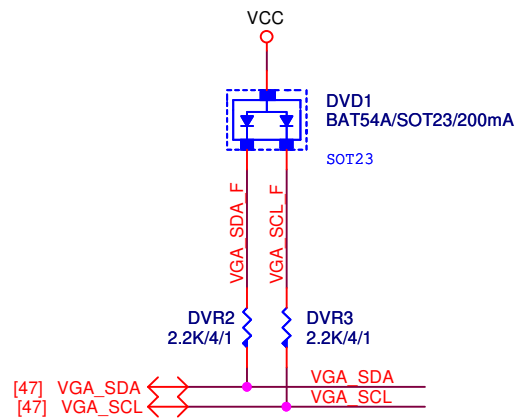


LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

DP HPD



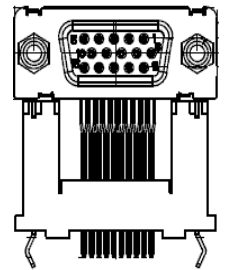
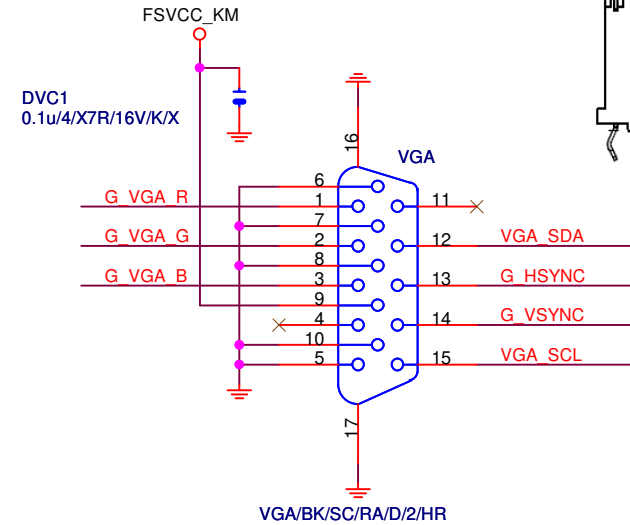
VGA SIGNAL R2.0



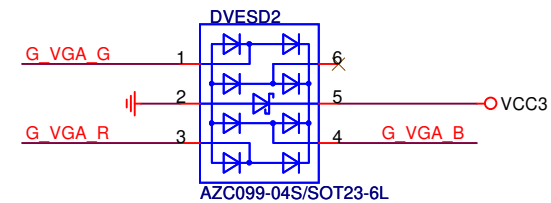
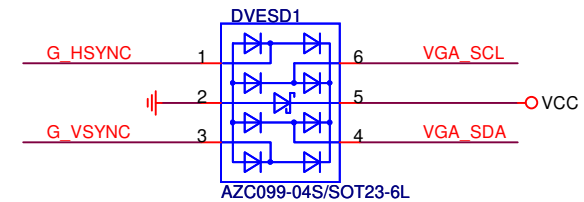
Close to Filter

FOR EMI

VGA CONN. 架高型VGA (BLACK)



VGA ESD



Gigabyte Technology			
Gigabyte Technology			
DP-VGA RTD2168			
Title	B560M DS3H		
Size	Document Number	Rev	1.0
Custom	B560M DS3H		
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8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

8	7	6	5	4	3	2	1
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8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

8	7	6	5	4	3	2	1
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8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

8	7	6	5	4	3	2	1
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8	7	6	5	4	3	2	1
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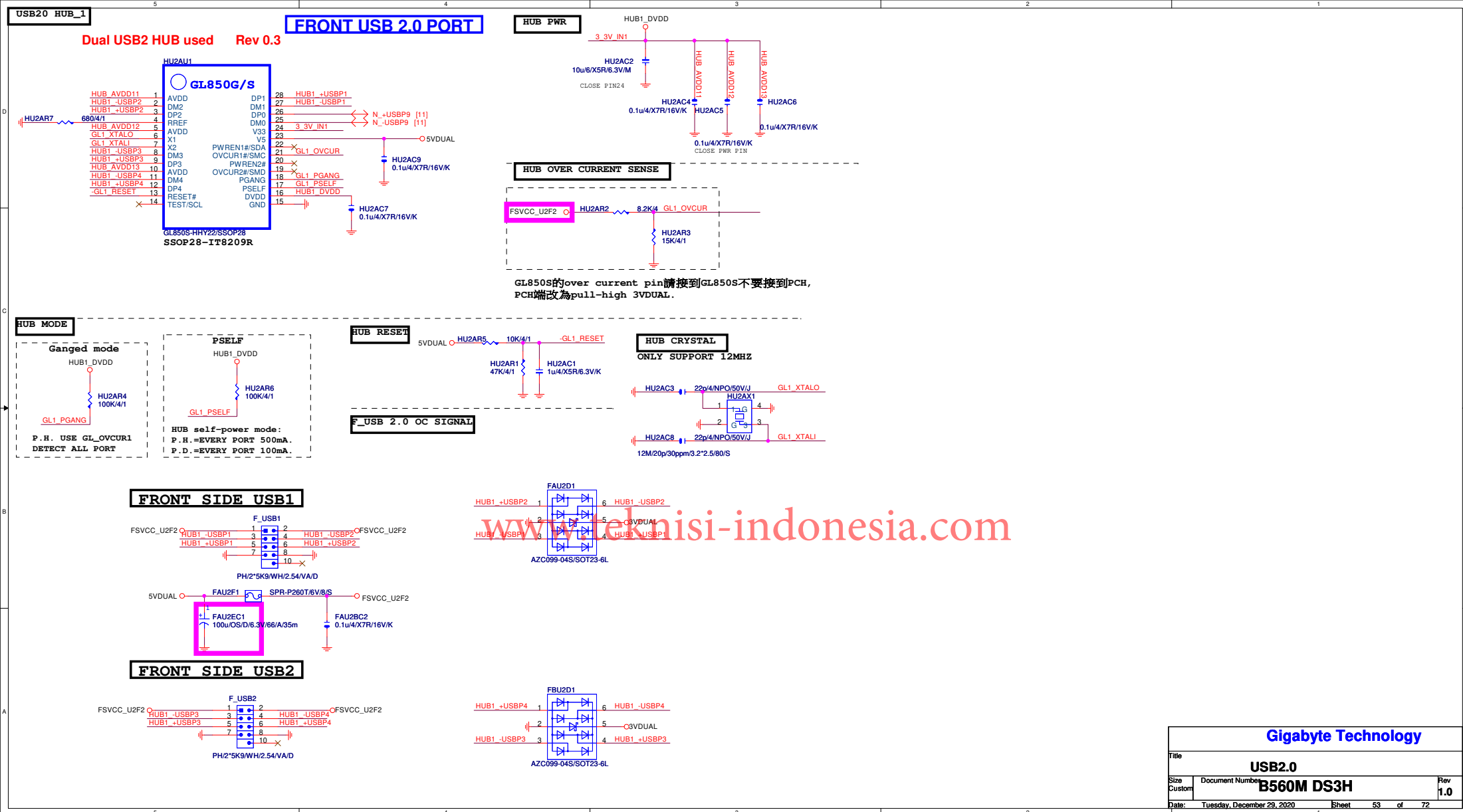
8	7	6	5	4	3	2	1
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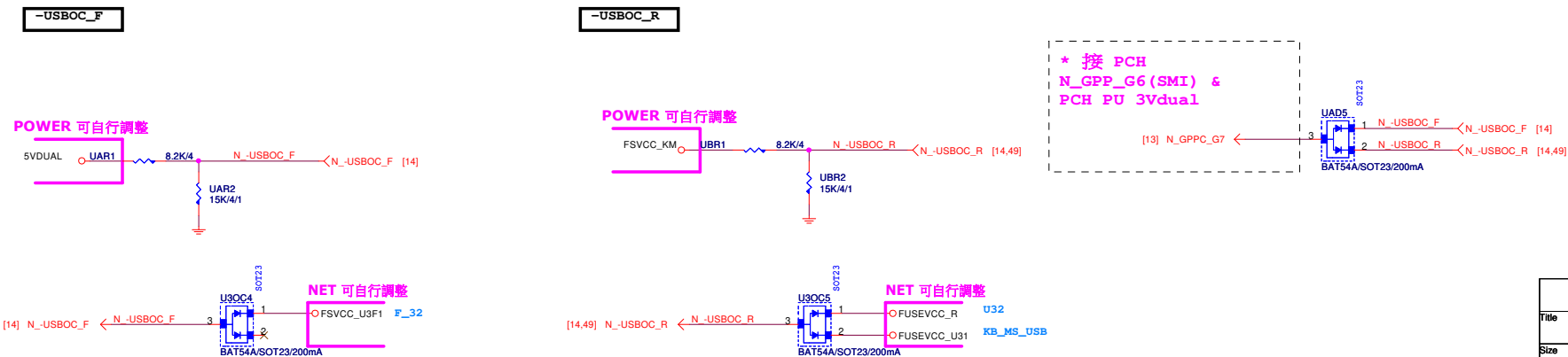
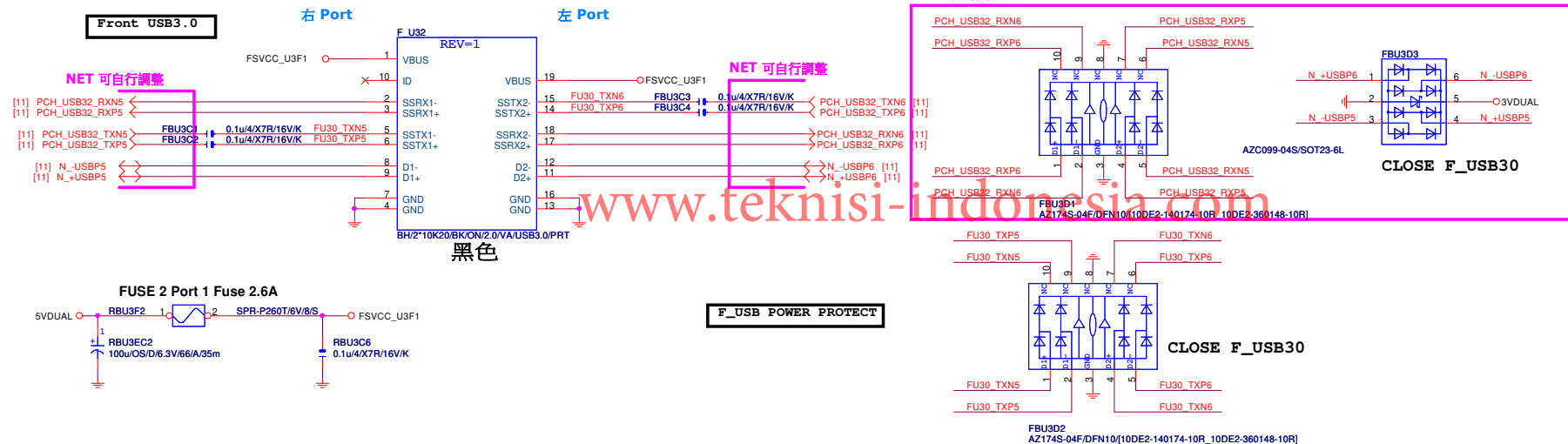
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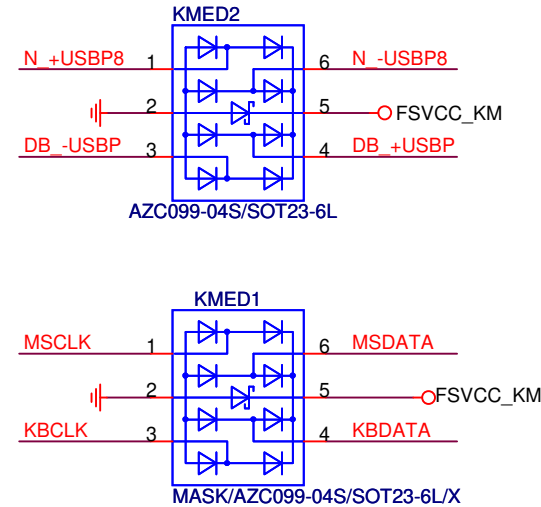
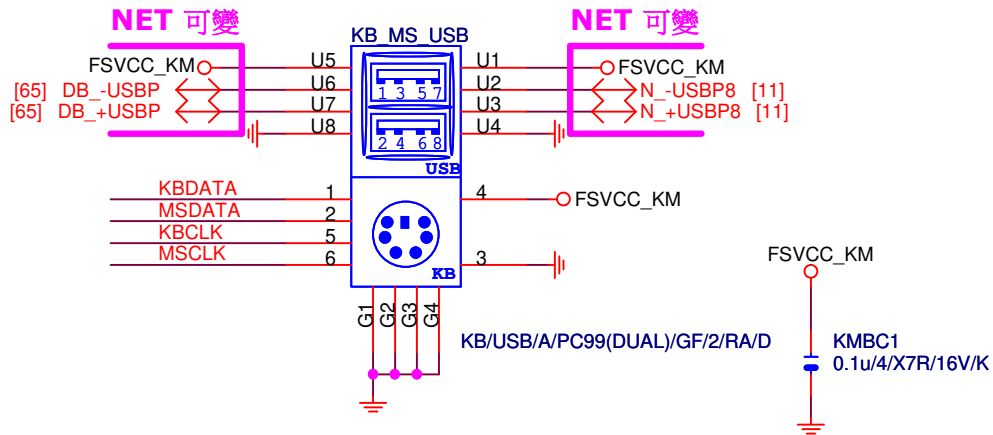


8	7	6	5	4	3	2	1
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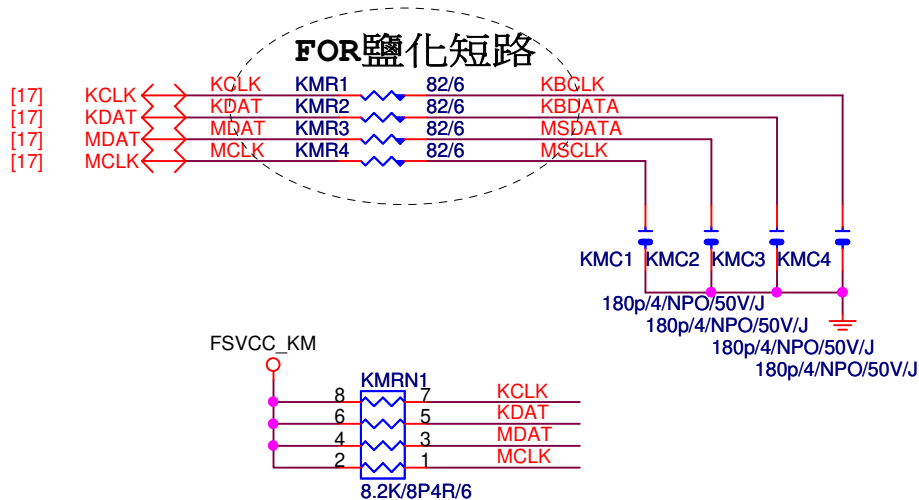
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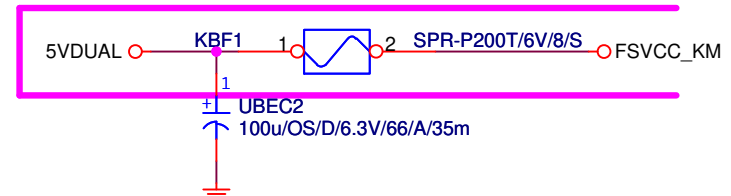


KB_MS_USB DAMPING/PU



KB_MS_USB PWR

NET 可變, 與其他USB SHARE



USB OC PROTECT

Gigabyte Technology

Title

KB_MS_USB30

Size

Document Number

B560M DS3H

Rev

1.0

Date:

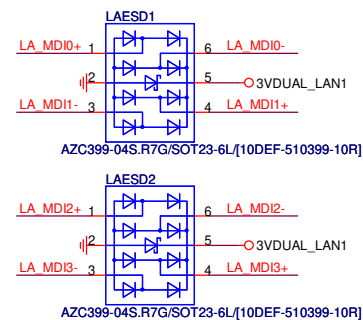
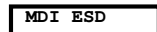
Tuesday, December 29, 2020

Sheet

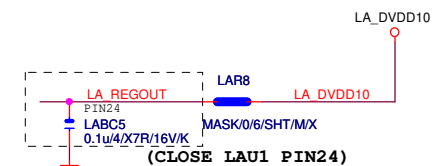
55

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72



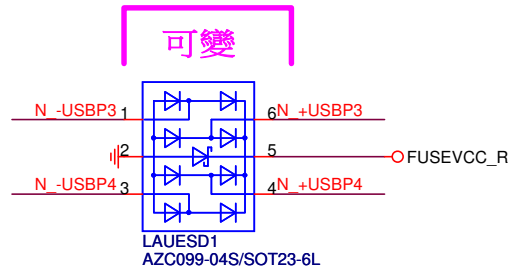
LAN POWER



<i>Gigabyte Technology</i> <i>Realtek RTL8111G</i>			
Title			
Size	Document Number		Rev
Custom	B560M DS3H		1.0
Date:	Tuesday, December 29, 2020	Sheet	57 of 72

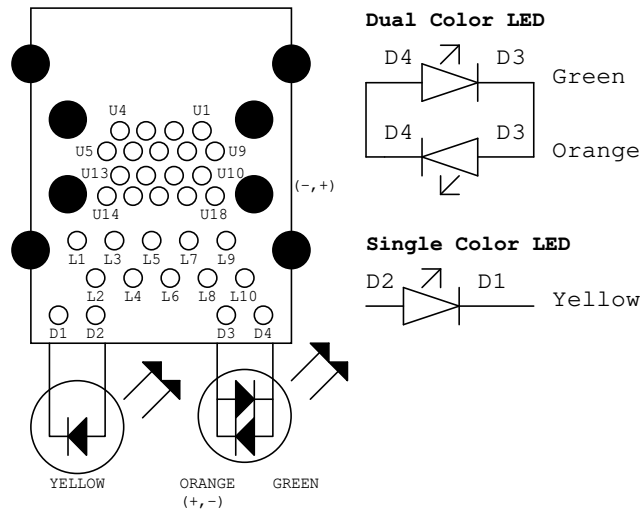
USB30_LAN CONNECTOR R2.01

RMA ESD PROTECT note:可變更USB NAME

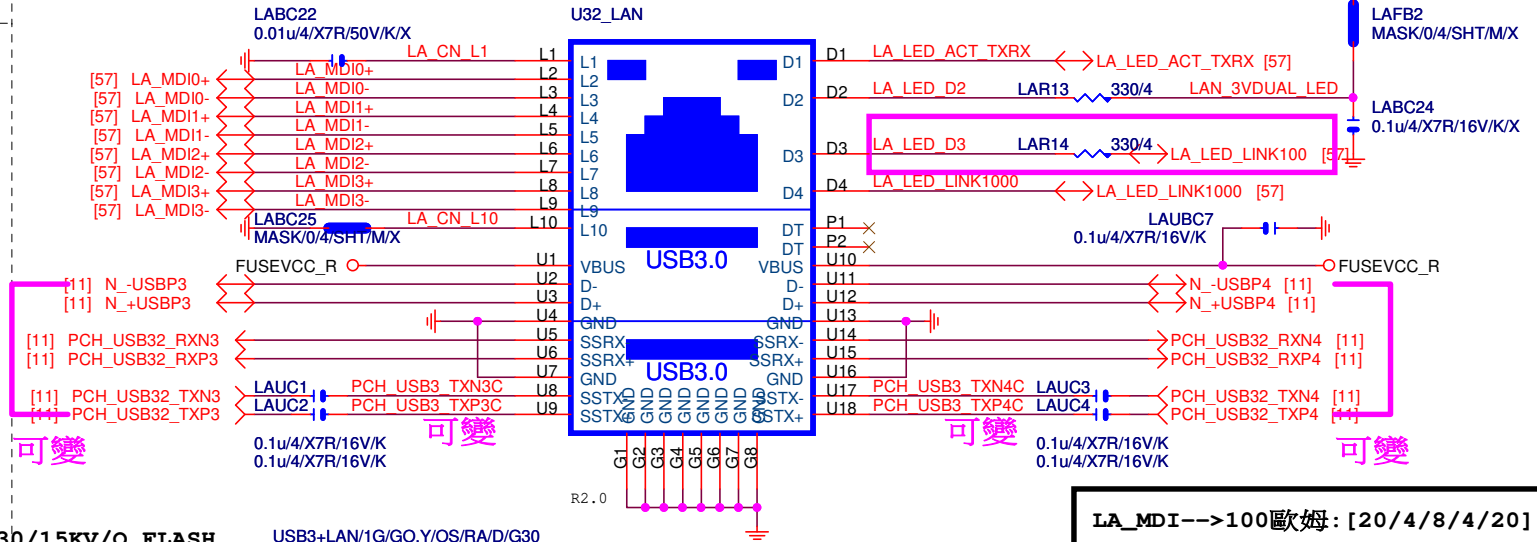


USB上白下藍:USB3+LAN/1G/GO,Y/OS/RA/D/G30/15KV/Q FLASH

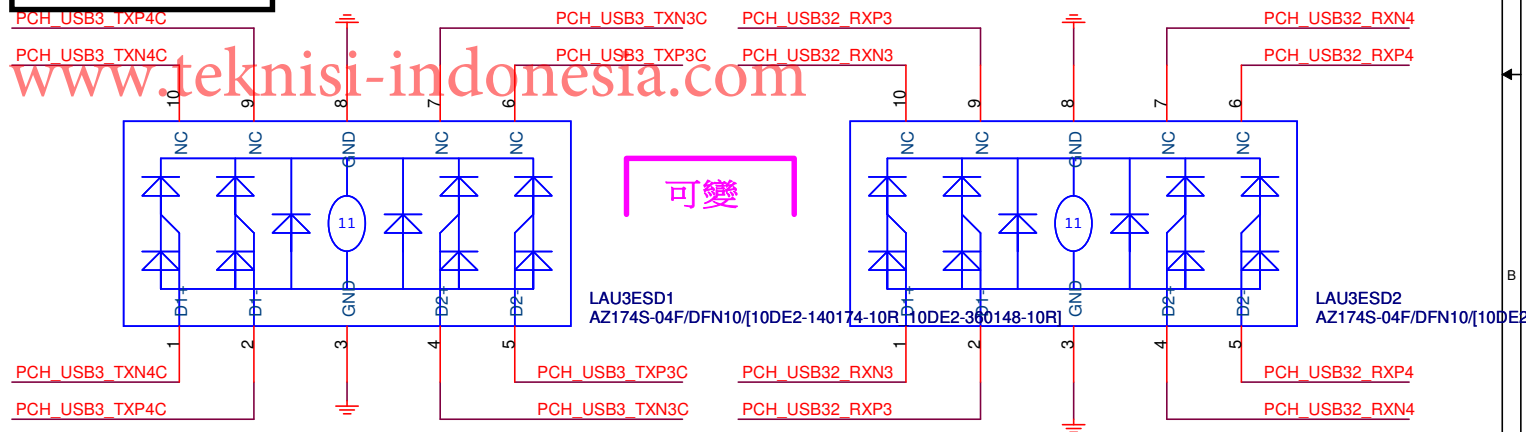
USB30_LAN LAYOUT示意圖



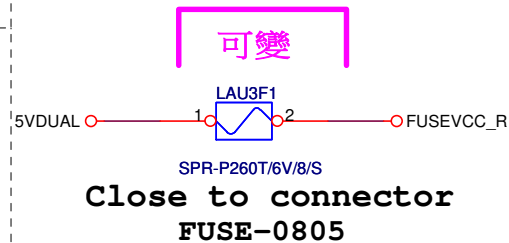
USB_LAN CONNECTOR [RTL8111G] note:可變更USB NAME



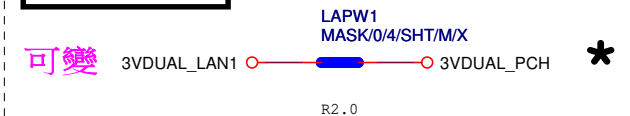
RMA ESD PROTECT note:可變更USB NAME



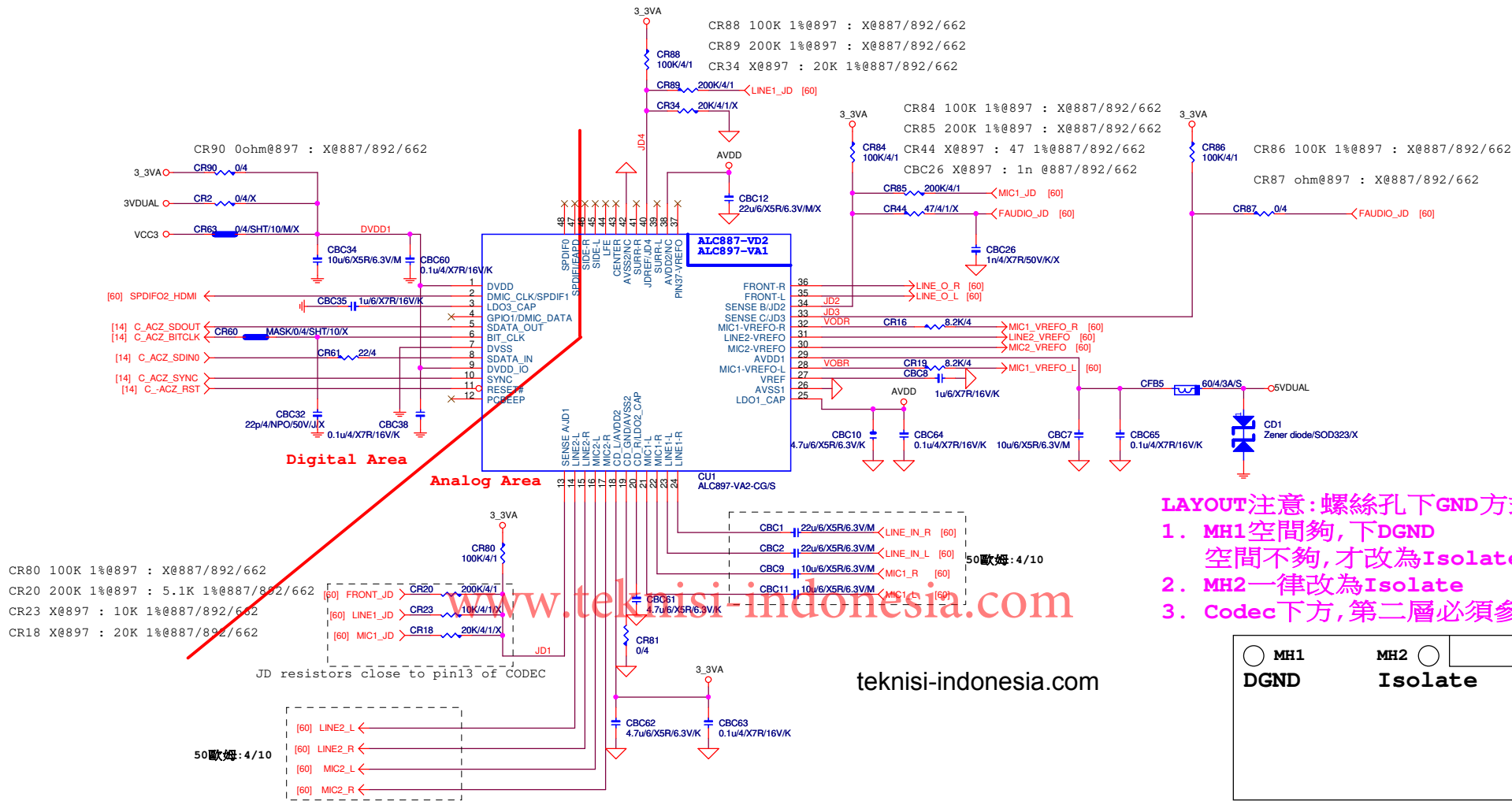
USB POWER note:可變更FUSE



LAN POWER note:lan power連接及電流



Gigabyte Technology			
LAN CONNECTOR-RTL8111G			
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BOM OPTION : 1. Chemicon音效電容
2. 金屬外罩 Reserve (LAYOUnT上件與否, 依照各Model spec)
3. LED Reserve (上件與否和LED顏色, 依照各Model spec)

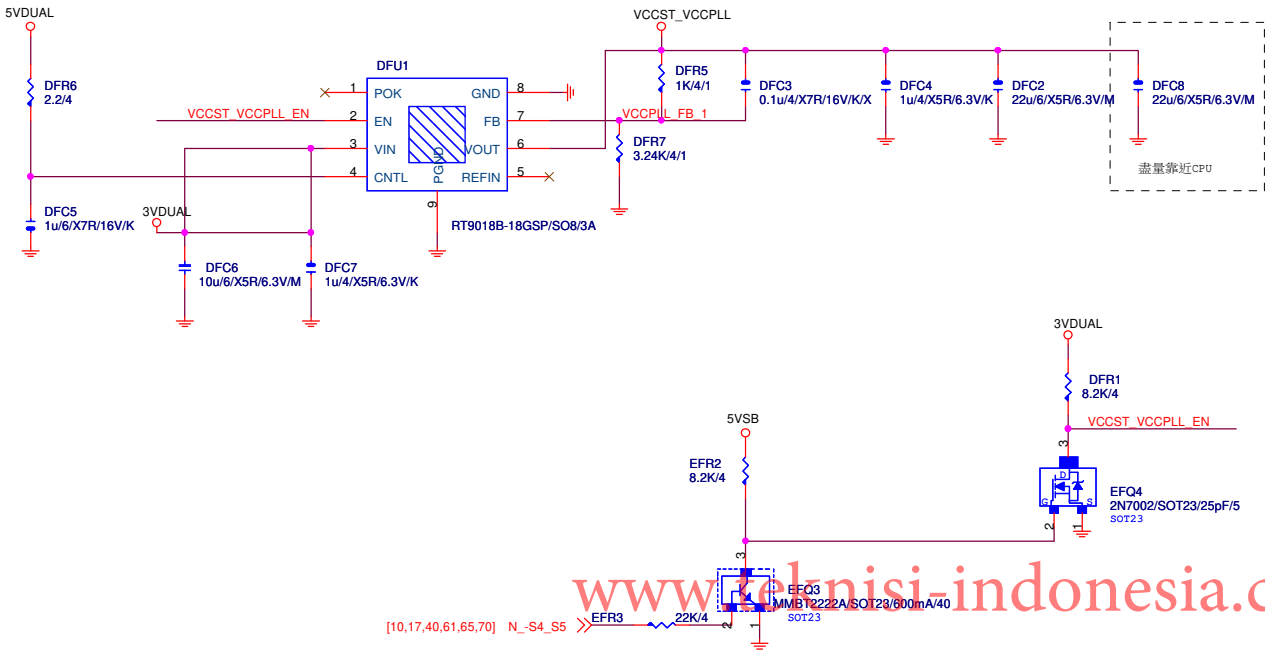


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Title			
CPU POWER-1			
Size	Document Number		Rev
Custom	B560M DS3H		1.0
Date:	Tuesday, December 29, 2020	Sheet	61 of 72

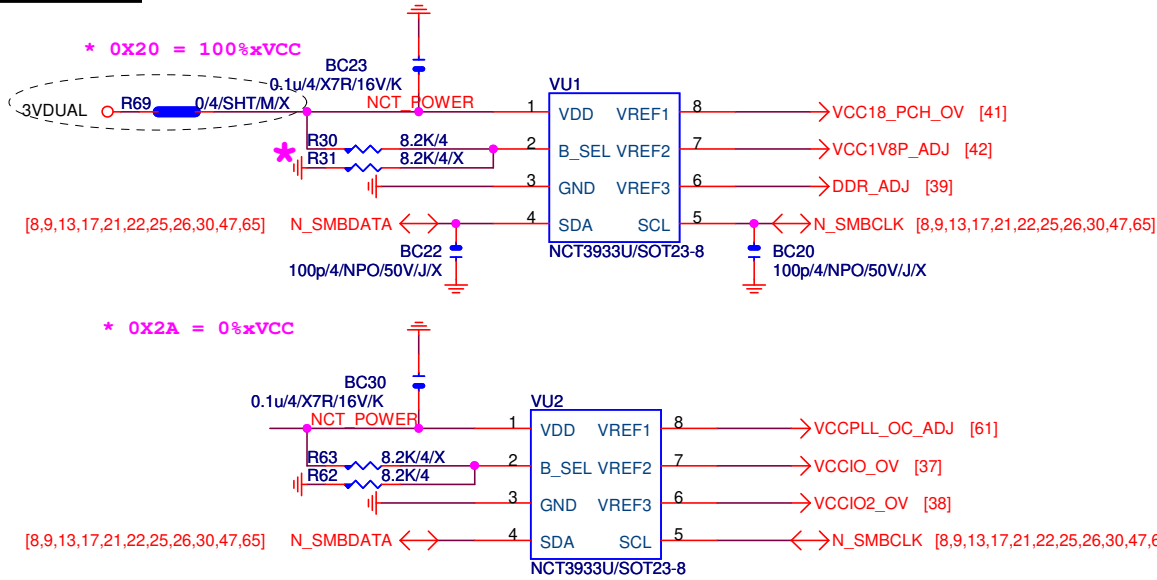
VCCST_VCCPLL 替換原先MOS開關線路



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GIGABYTE™			
Title CPU POWER-2			
Size Custom	Document Number B560M DS3H		Rev 1.0
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B560

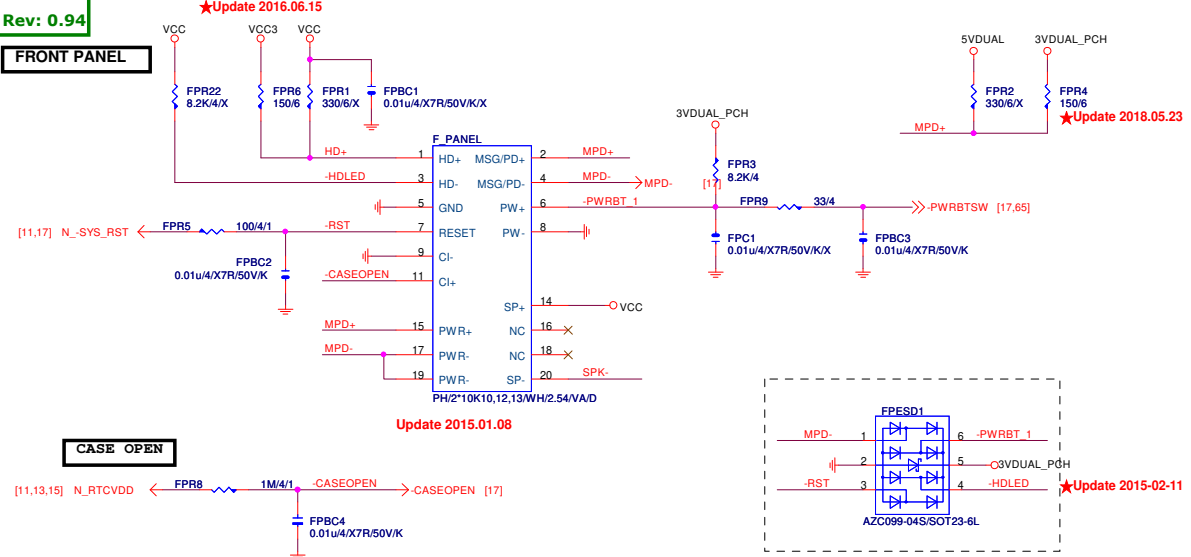


NCT3933	0X2A	0X20
VREF1	VCC18_PCH	VCCPLL_OC
VREF2	VCCIO	VCC1V8_PRIM
VREF3	VCCIO2	VDDQ

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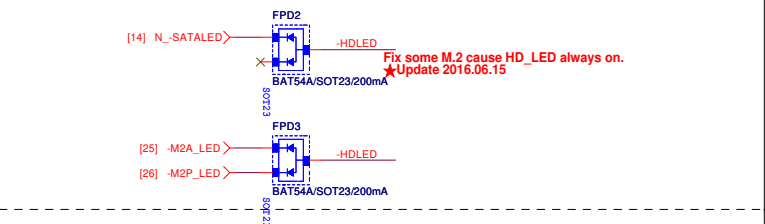
Gigabyte Technology		
CPU CORE VR-2		
Size Custom	Document Number	Rev
	B560M DS3H	1.0
Date:	Tuesday, December 29, 2020	Sheet 63 of 72

FRONT PANEL

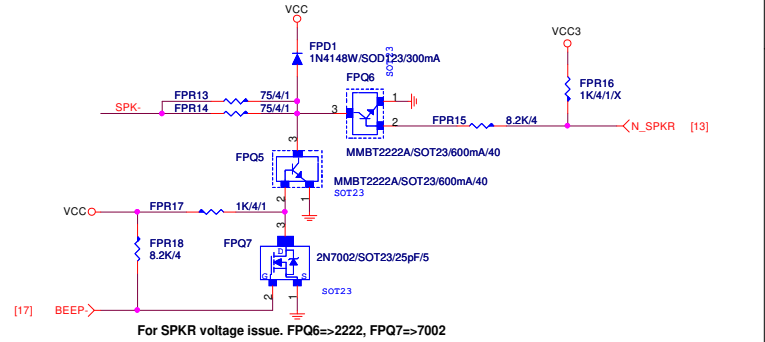


FRONT PANEL SHORT

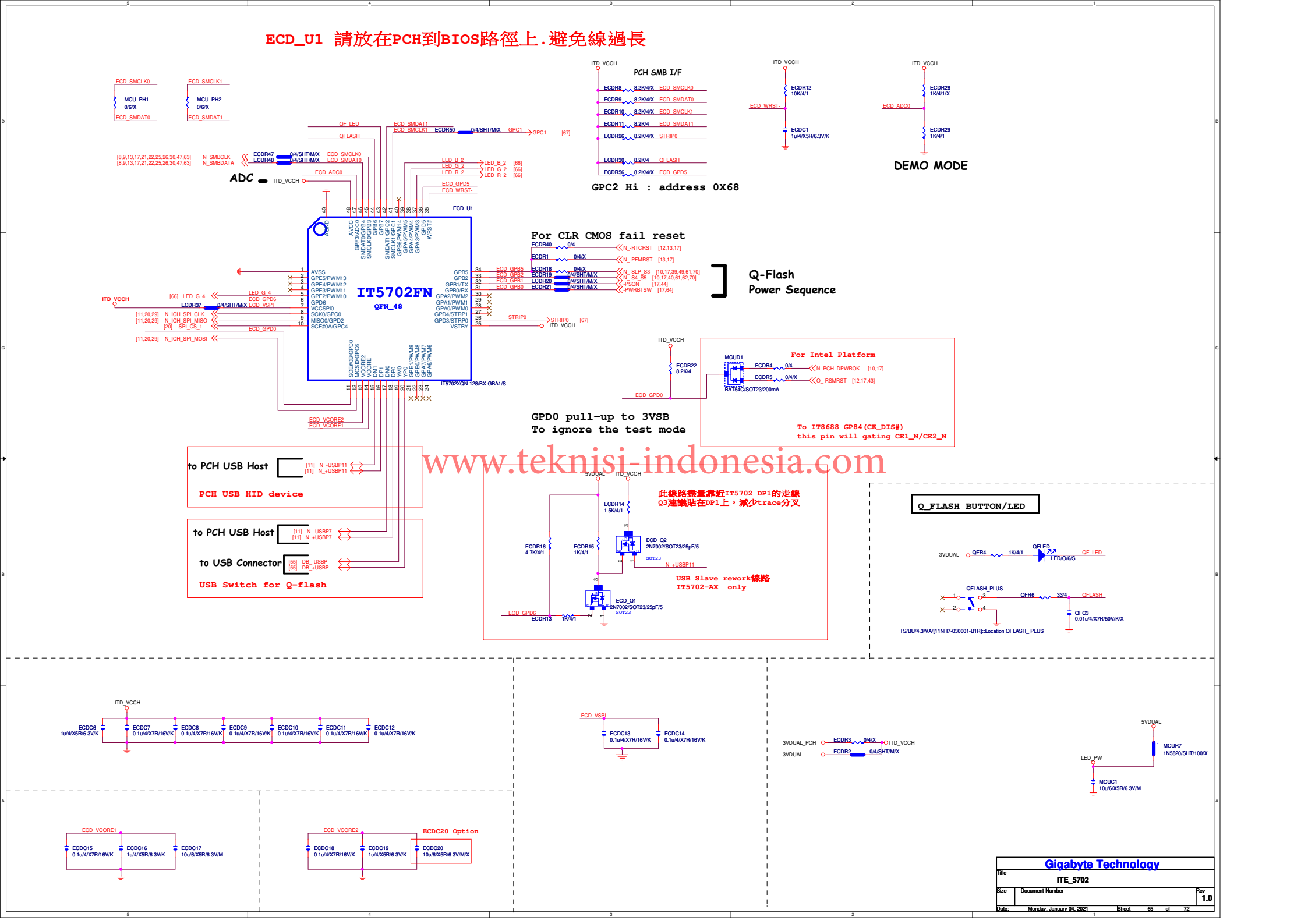
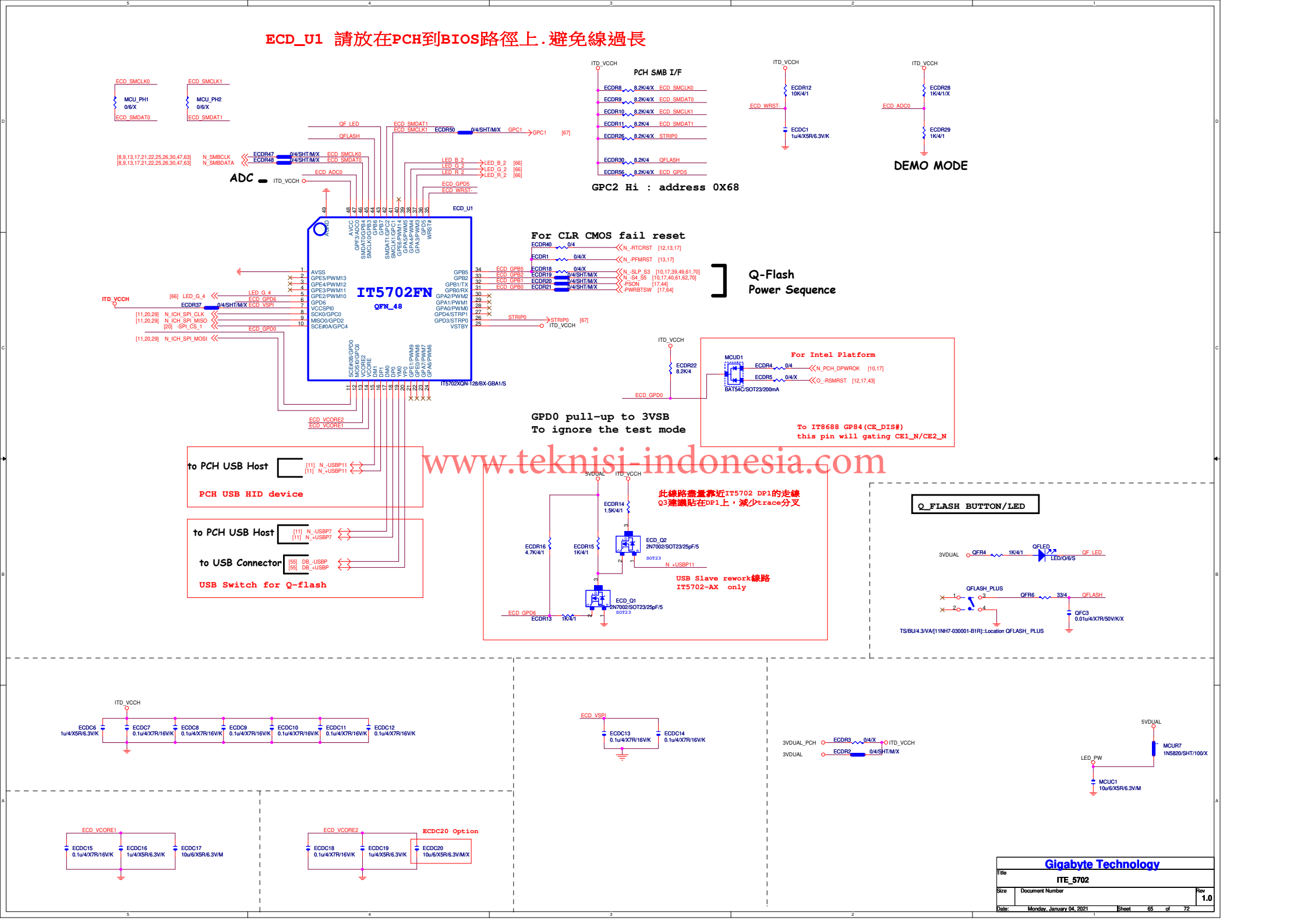
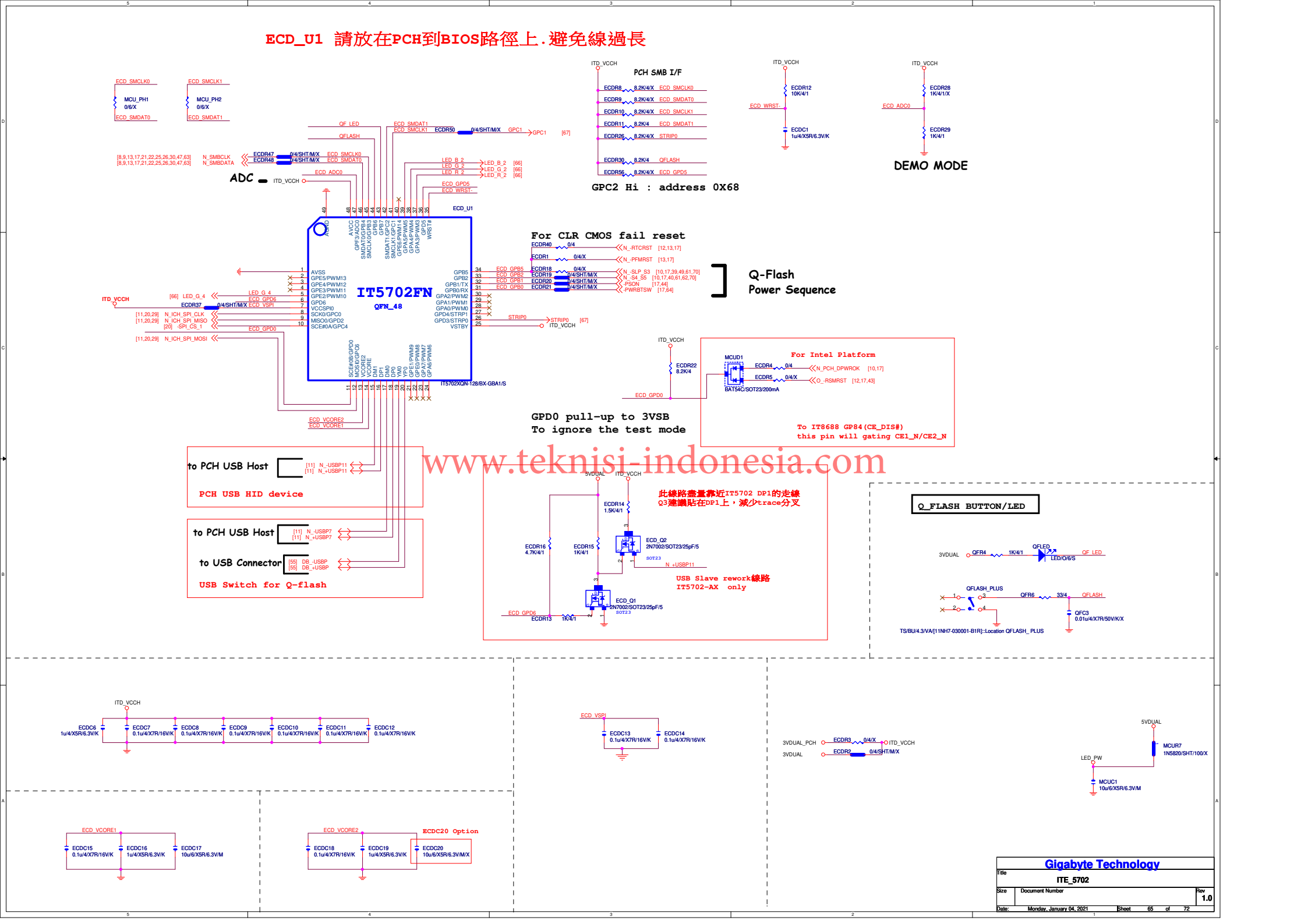
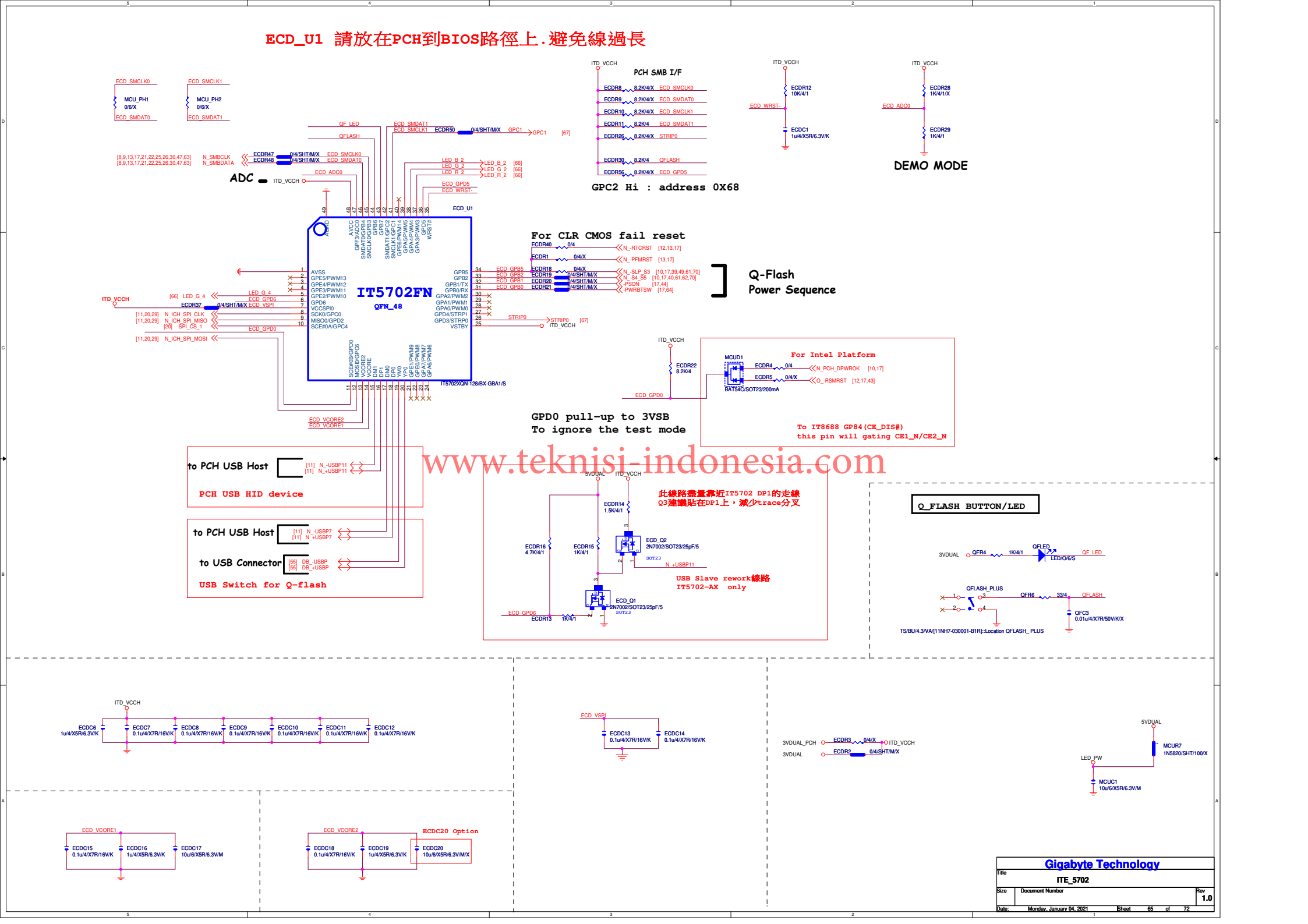
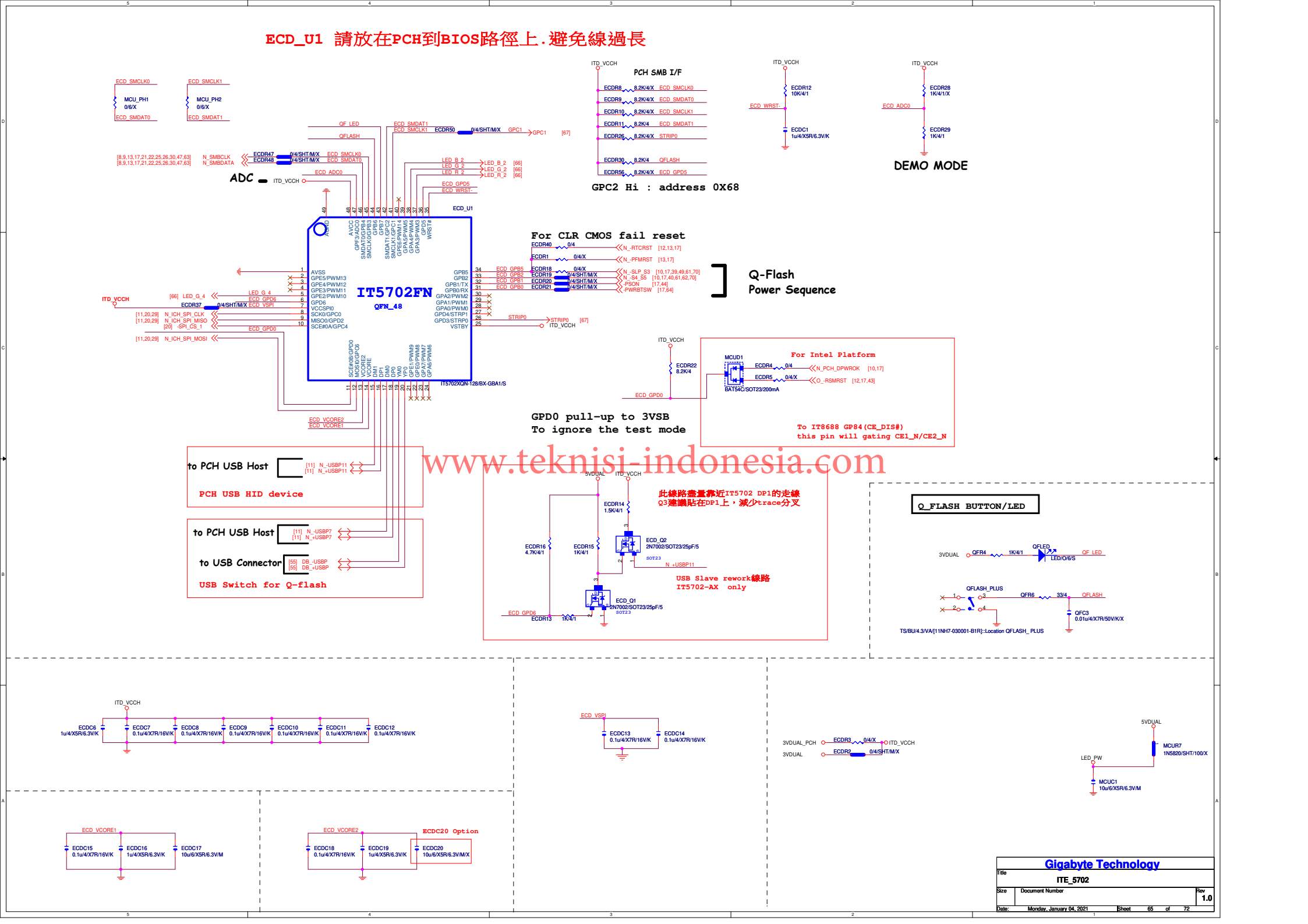
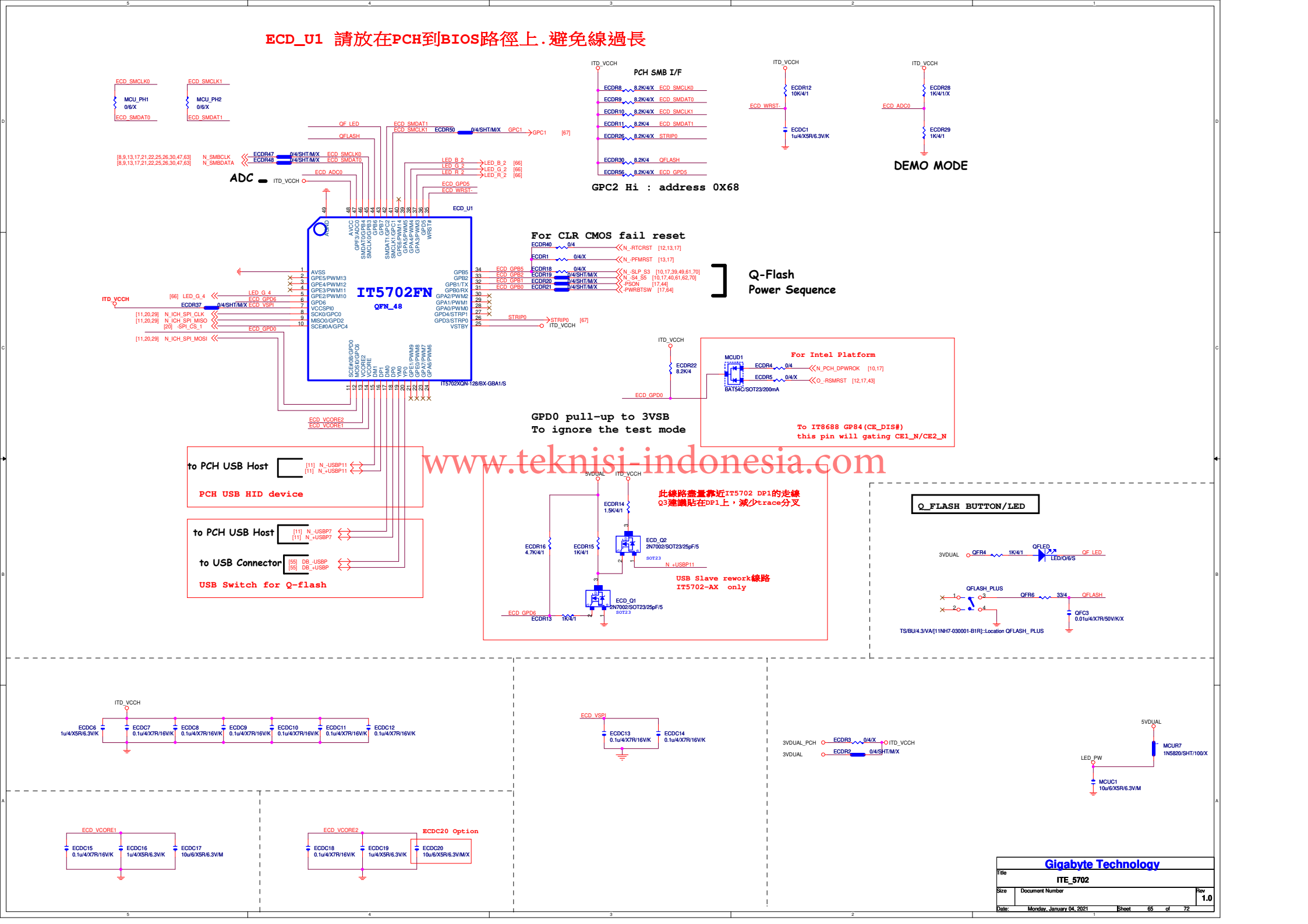
SATA/M.2 LED



SPKR W/O EC



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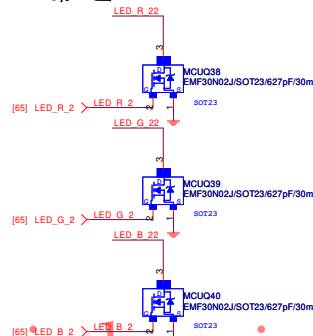
[illegible]

第三區 LED

第四區 LED

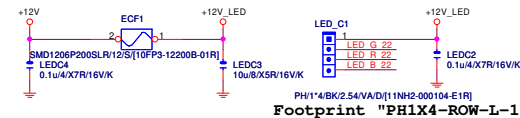
第五區 LED

第二區 LED CONTROL



燈條 LED (LED_C1放在PCB左邊板邊位置)

燈條 LED (LED_C2放在PCB右邊板邊位置)

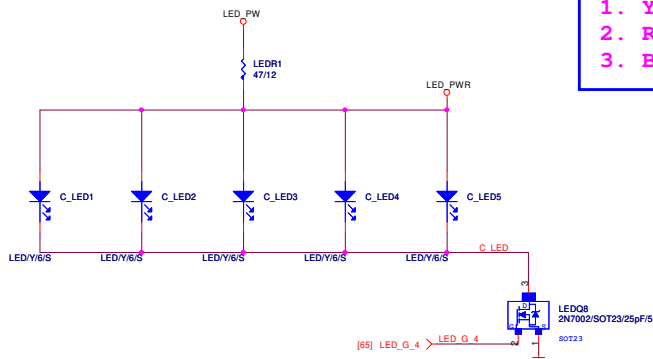


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第四區 LED CONTROL

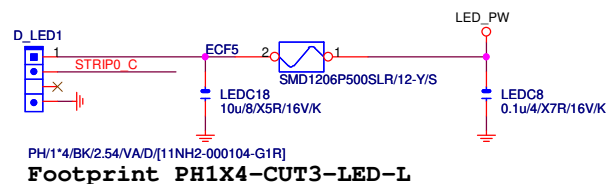
BOM OPTION :

1. YELLOW LED : LED/Y/6/S
2. RED LED : LED/R/H/0603/S
3. BLUE LED : LED/B/6/S



第六區 LED (靠近左上板邊位置)

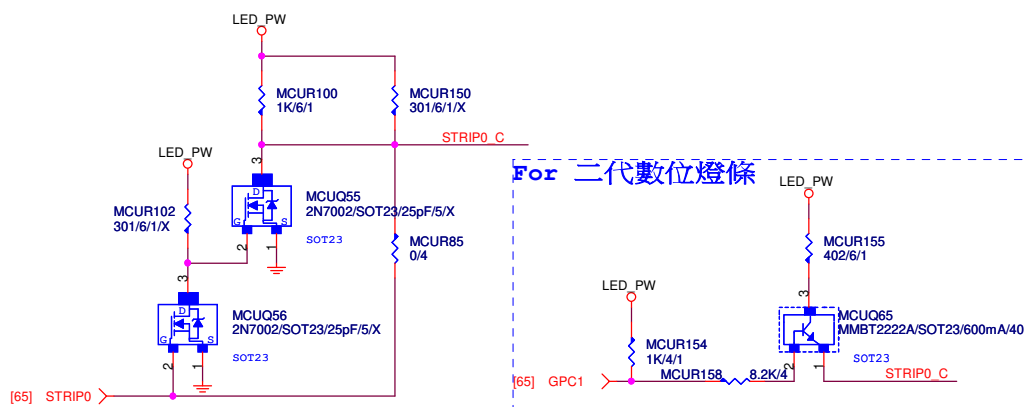
Digital LED Strip1



第七區 (靠近右下CPU板邊位置)

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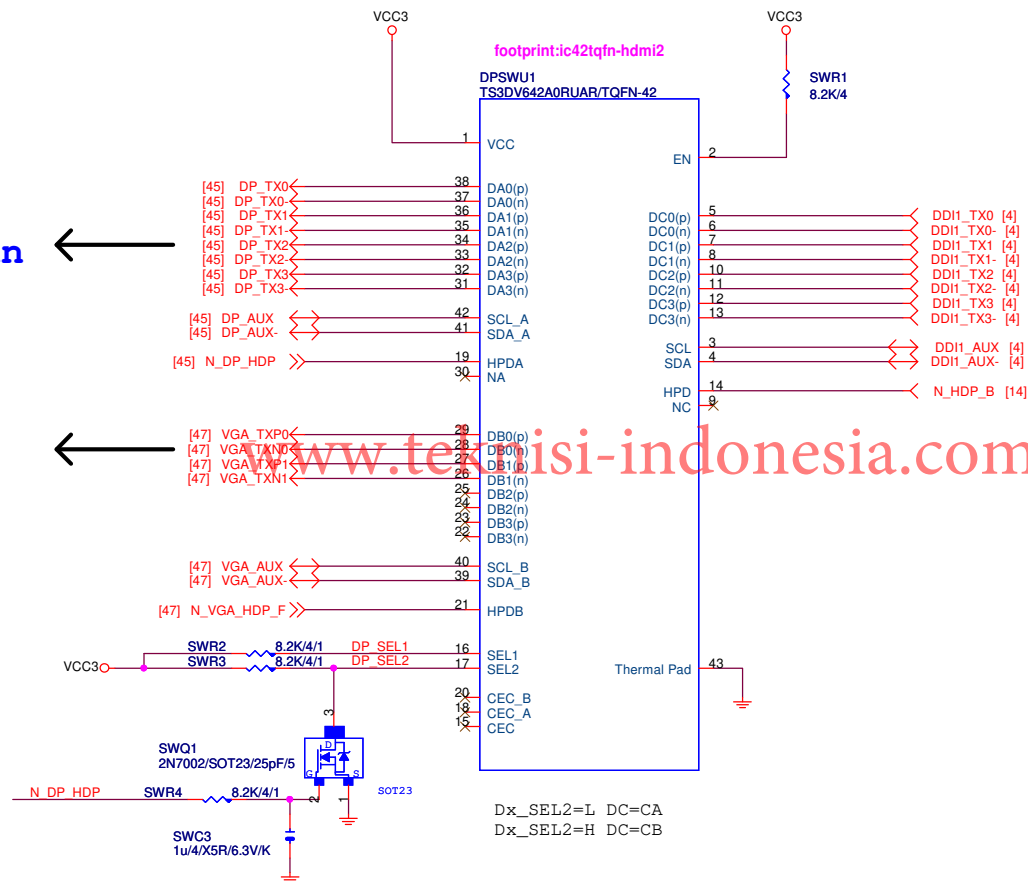
燈條 Level shift



GIGABYTE™

Title		
D_LED1/D_LED2		
Size	Document Number	Rev
Custom	B560M DS3H	1.0
Date:	Tuesday, December 29, 2020	Sheet 67 of 72

To DP Conn

To D-SUB
(RTD2168)

CPU DDI1

1. DEFAULT: D-SUB VGA (RT2168) --SW CB (SEL2=HI)
2. 當DP HOTPLUG (DP_AUX_GND-->LOW) 插入, 切到DP; --SW CA (SEL2=LOW)

Gigabyte Technology
VGA SWITCH

Title		
Size B		
Document Number	B560M DS3H	
Date:	Tuesday, December 29, 2020	Sheet 68 of 72
Rev	1.0	

CLOSE SIOEMIC1
100p/4/NPO/50V/J/X

[10,17,39,40,61,65] N_SLP_S3 ←

EMIC2
100p/4/NPO/50V/J/X

[10,17,40,61,62,65] N_S4_S5 ←

CLOSE PCHEMIC4
100p/4/NPO/50V/J/X

[4,10] N_CPUPWROK ←

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Title

EMI/ESDSize
A

Document Number

B560M DS3H

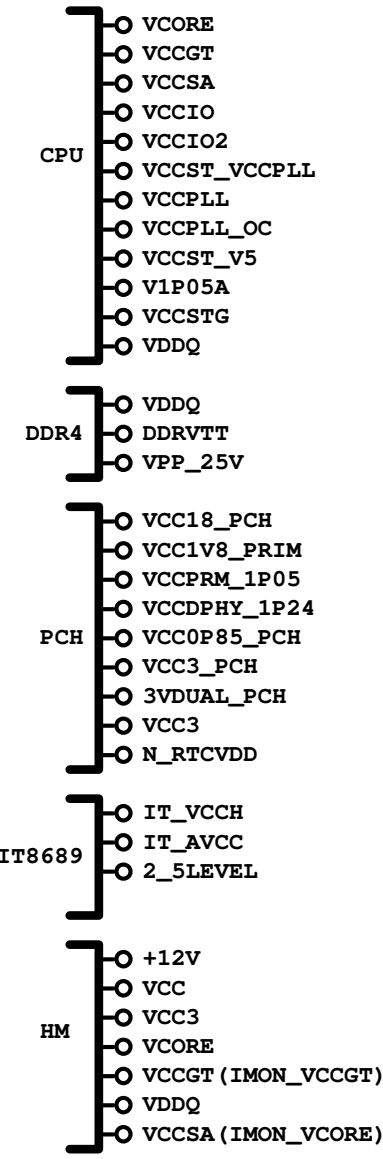
Rev

1.0

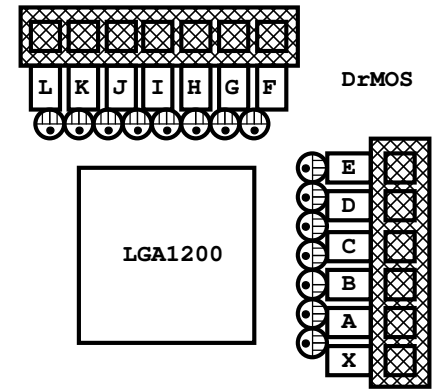
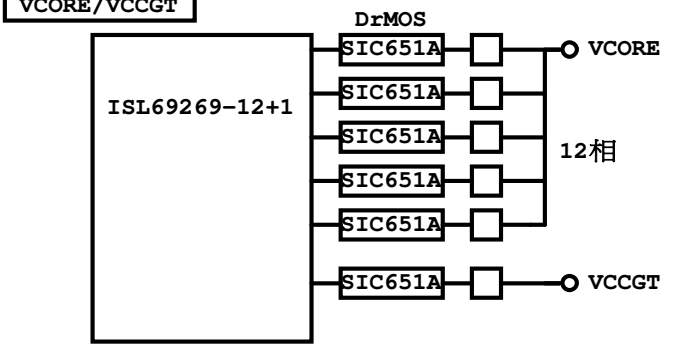
Date: Tuesday, December 29, 2020

Sheet 70 of 72

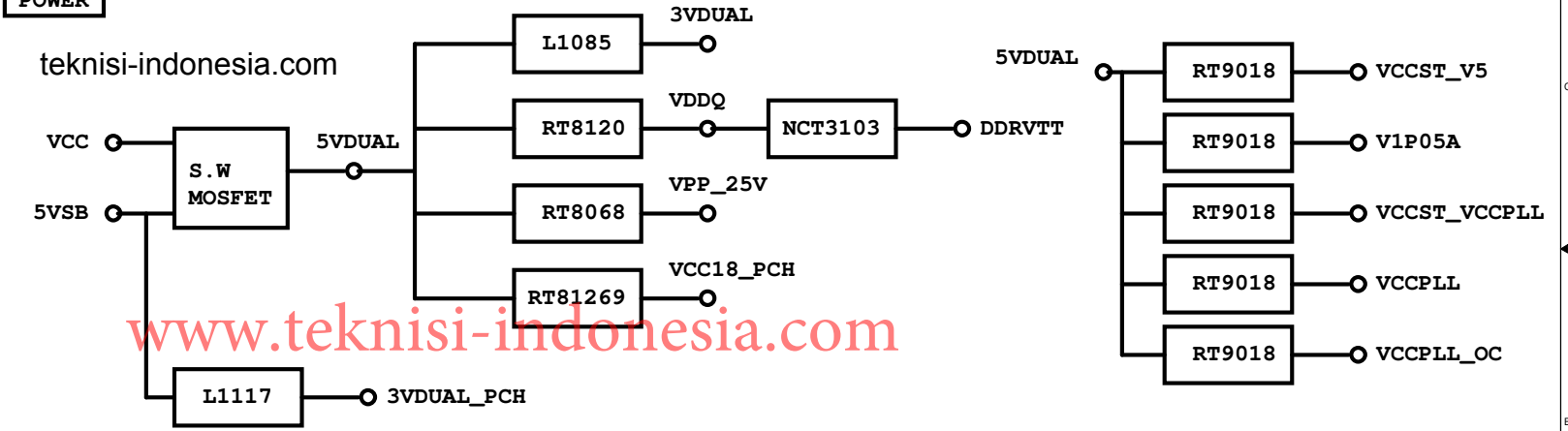
POWER BLOCK MAP



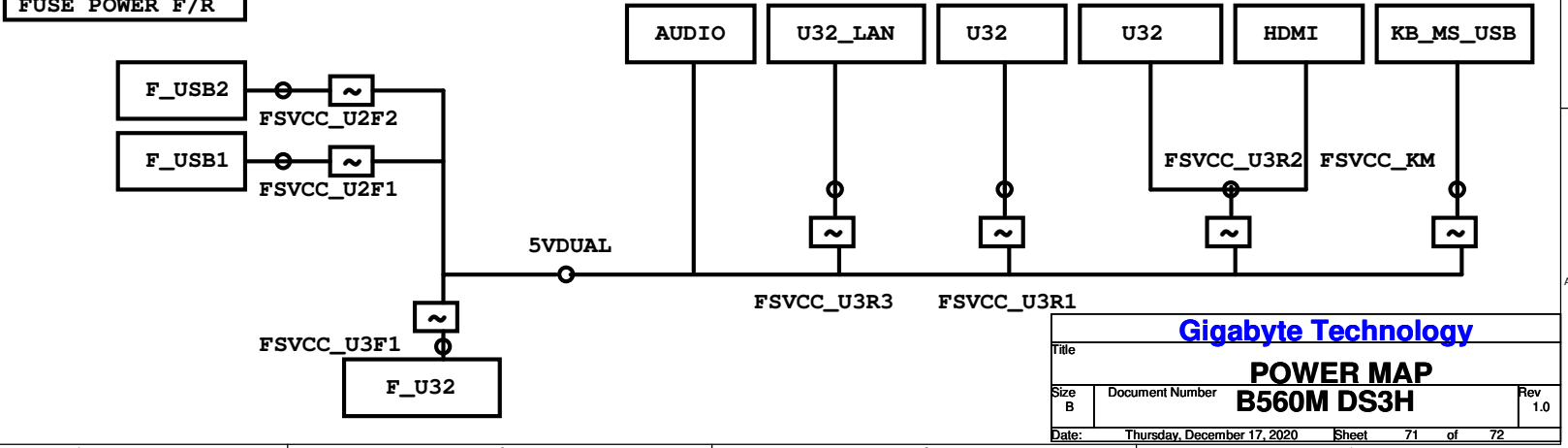
VCORE/VCCGT



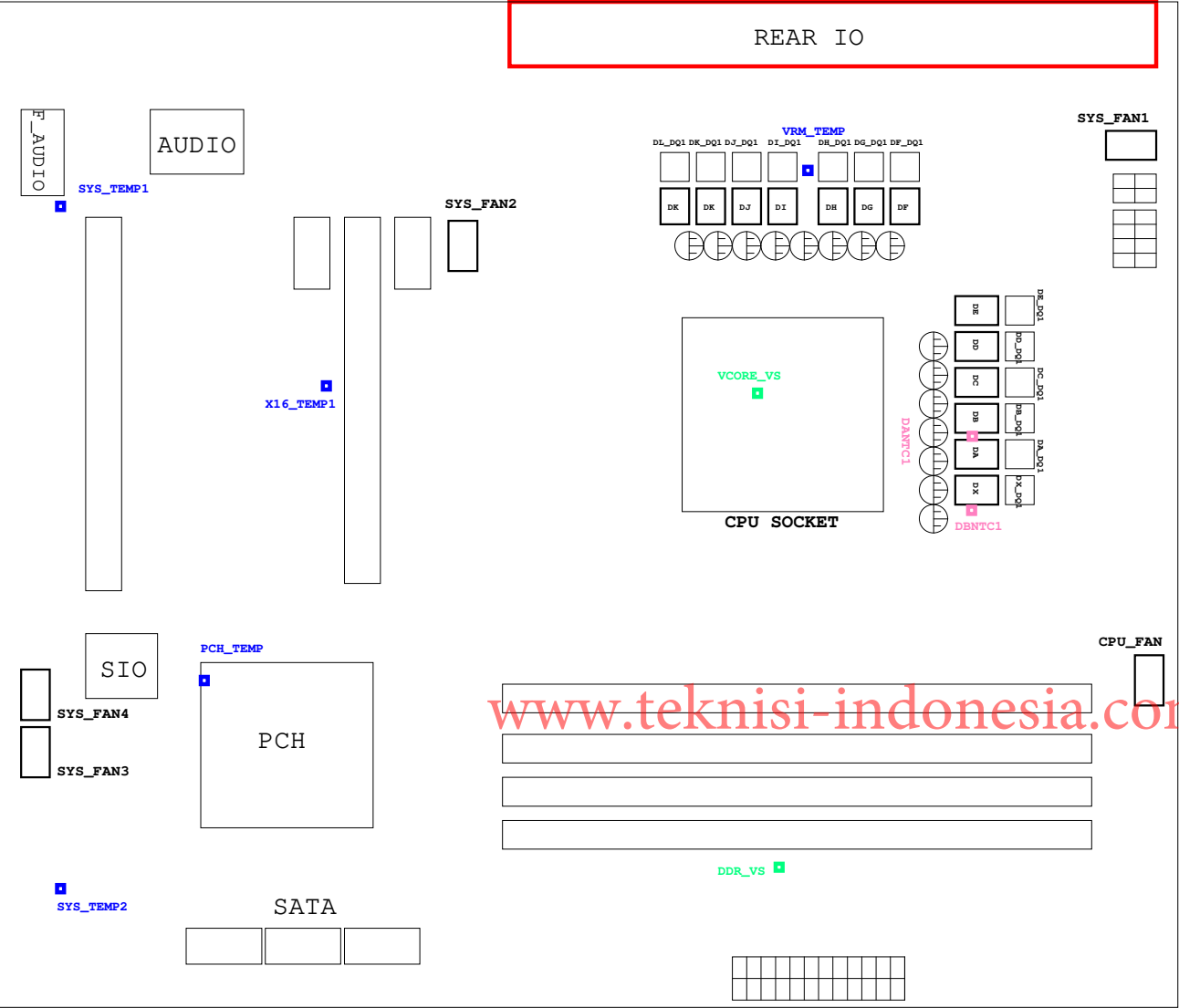
POWER



FUSE POWER F/R



Gigabyte Technology			
Title			
POWER MAP			
B560M DS3H			
Size	Document Number	Rev	1.0
B			
Date:	Thursday, December 17, 2020	Sheet	71 of 72



熱敏電阻	擺放靠近位置	走線方式
DANTC1	DA_DL2	Differential
DANTC2	DA_DQ3	Differential
DANTC3	DM_DQ2	Differential
DANTC4	DM_DL1	Differential
VRM_TEMP	DC_DQ1	N/A
X16_TEMP1	PCIEX16	N/A
PCH_TEMP	PCH	N/A
SYS_TEMP1	F_AUDIO	N/A
SYS_TEMP2	F_PANEL	N/A

- SIO RS
- PWM RS
- SIO VIN



FAN